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SYSTEM ORGANIZATION OF THE DYSEAC

A. L. Leiner and S. N. Alexander
National Bureau of Standards
Washington, D.C.

SUMMARY—The DYSEAC is a complete general-purpose h-speed digital computer utilizing the same basic electronic cuit elements as those in SEAC. In the DYSEAC, however, se basic building blocks have been organized into a more erful system for controlling and responding to auxiliary ices. Communication between these auxiliary devices and DYSEAC (or between the DYSEAC and the persons operat- it) can take place at any time, on a completely unscheduled is, at the instigation of either the computer or the external ld, or both acting jointly. The system features which en- e such impromptu interchanges of information to occur are cribed in this paper.

INTRODUCTION

The current trend toward the automatization of indus- al and commercial operations is opening new areas of erest in which the techniques developed for digital ipment could be exploited. In particular, the unusual xibility and speed inherent in these techniques could utilized for automatizing a number of complex indus- l control and supervisory tasks. Unfortunately, explor- on of these new areas cannot be undertaken efficiently h existing digital computers because of the strong s in the design of currently operating equipment ard scientific and engineering tasks. If, however, the ernal flexibility of machines of this general type were tched by equally flexible means for keeping them in tinual communication with devices external to them, ital computers could be used to advantage both in trol systems for industry and in information-processing tems for handling the mass paper work of business.

As an example, before digital computers can be cessfully incorporated into the often-predicted utomatic office" of the future, such equipment must sess ready means for sending intelligence to and eiving intelligence from a variety of external devices forming many diverse functions. Some of these devices l have to store, tabulate, file, convert, display and se information; still other devices will have to actuate chanisms such as servo equipment in response to nals sent out by the computer as a result of informa- n being processed within it. The computer will have irect all these devices and coordinate their activities o an ensemble operation.

Indeed, to achieve the full effect of an ensemble ration, the system needs to have the characteristics a generalized feedback loop. That is, the computer st not only exert control over these external devices, they in turn must be capable of calling for alteration the course of action of the computer. Such requests enter the computer as special signals or information transfers from the external devices.

This feedback arrangement can be used to introduce human monitoring and selective intervention into the normal operation of the system. In its simplest form, pertinent information is displayed to the human operator who can elect to respond by actuating other external devices that supply the computer with either new data or instructions.

The DYSEAC system was planned with just such requirements in mind and is capable of exploring many of these new areas. The central core of the DYSEAC is a complete general-purpose high-speed digital computer utilizing the same basic circuit elements as those in SEAC. In the DYSEAC, however, these basic building blocks have been organized into a far more powerful system for controlling and responding to auxiliary external devices. Since the supervisory and control tasks for which this machine was planned did not require marked increase in computing speeds, the arithmetic powers of the DYSEAC have been only moderately expanded over those in SEAC by reorganizing the computation-control facilities to carry out new and improved arithmetic operations. Major design emphasis was placed, instead, on versatility of control facilities and on latitude for expansion of the installation.

It was deemed important to provide for future expansion of the high-speed internal storage capacity, in case this becomes important for a particular application. Accordingly, the system has been provided with convenient means for supplementing the initial memory capacity of 512 words with additional storage units up to a total capacity of 4096 words. A more significant provision for expansion, however, concerns the annexation of a wide variety of specialized external devices.

The kind and extent of the external devices to be added will necessarily depend on the particular application which is being explored. Nearly all tasks need some printing and external storage facilities; hence, the initial installation will have a directly connected electromechanical typewriter and one or more magnetic wire cartridges for speedy loading and unloading of the machine. External storage in the form of magnetic tape equipment is also to be included initially in order to handle the more usual computing and data-processing tasks. More demanding tasks requiring somewhat faster access to a rather large volume of data will probably lead to the annexation of one or more magnetic drum units. Still more extensive problems concerned with means for handling masses of paper work will probably lead to the

subsequent addition of experimental magnetic disk memory assemblies and experimental versions of the automatic magnetic file. For the exploration of real-time problems, including simulation and control aspects, it will be necessary to annex input and output converters to permit translation of information back and forth from digital to analog form. For example, digital-to-analog conversion is used when visual display of information stored inside the computer is provided externally by means of special cathode-ray tube devices. This listing of external devices includes only those for which serious attention and development are already in progress.

One further device that may be attached to DYSEAC for special experiments is SEAC itself. Since the two machines employ the same digital language, this attachment can easily be made through their regular input-output terminals. By use of a coordinated pair of programs, the two machines can be made to work together in common harness on a number of interesting and potentially useful tasks. Indeed, this mode of operation can, by the application of available technology, be extended to a widely dispersed group of information-processing machines that are interconnected by means of a communication network. With suitable feedback facilities and correlated processing programs these machines could even engage in cooperative tasks for which the supervisory functions are transferred back and forth, as the need arises, among the several machines in the network. These new approaches to the problem of automatizing industrial and commercial operations are reasonable extrapolations of current trends and can be expected to lead to practical results if vigorously pursued.

SYSTEM FEATURES

The system specifications for DYSEAC are summarized briefly in Table 1. While some of these specifications are similar to those in SEAC or are expansions of SEAC counterparts, many are entirely new. Most significant of the new provisions are the Special Operating Features listed at the end of the table. These features are designed to facilitate communication between the DYSEAC and the outside world (i.e., between the machine and the persons operating it or the external devices subsidiary to it) and enable impromptu interchanges of information to occur between them at any time on a completely unscheduled basis. Furthermore, such interchanges can be instigated by either the machine or the outside world, or by both acting jointly.

There are three general properties which give the DYSEAC this versatility:

1. External-transfer operations, which transfer information between the machine and the external devices, are performed concurrently with internal computing operations; moreover, these transfers can refer directly to any area of the internal memory without restriction as to location or size.

2. The pace at which the work program is carried out within the machine can be automatically adjusted to

TABLE I

DYSEAC SYSTEM SPECIFICATIONS

GENERAL OPERATING CHARACTERISTICS

Basic repetition rate	One megacycle per second.
Data representation	Binary system; serial mode of representation.
Word length	Forty-four binary numerical digits plus one sign digit.
Instruction system	Three-address system in which a typical instruction word specifies the 12-digit address of first operand (α), second operand (β), and result of operation (γ). Successive instructions are generally located in consecutively numbered memory locations.
Memory	Mercury acoustic delay lines containing eight words each, with a maximum access time of 384 microseconds. Minimum capacity: 512 words, stored in a 64-line cabinet; maximum capacity: 4096 words, stored in eight such cabinets. Automatic parity-digit check of storage accuracy.

PERFORMANCE RATES OF BASIC OPERATIONS: (INCLUDING AVERAGE ACCESS TIME TO THE MEMORY)

Addition	0.9 millisecond	
Subtraction	0.9 millisecond	
Accumulate—and—Overflow-Check	0.7 millisecond	
Accumulate—and—Store	0.9 millisecond	
Summation	0.8 millisecond	(plus 0.05 millisecond per word)
Multiplication, major (rounded)	3.0 milliseconds	
Multiplication, minor	3.0 milliseconds	
Division	3.0 milliseconds	
Shift	1.1 milliseconds	(for half-word-length shifts)
Justify	2.0 milliseconds	(for half-word-length shifts)
Logical Transfer	0.9 millisecond	
Comparison, algebraic	0.7 millisecond	
Comparison, absolute	0.7 millisecond	
File, unconditional	0.4 millisecond	
Breakpoint-File	0.4 millisecond	
Input-Output	0.3 millisecond	(internal program time only)

SPECIAL OPERATING FEATURES

Internal program-control features	Dual counter-registers for program sequencing. Base-address and relative-address option.
Joint internal-external control features	Manual-monitor facilities. Breakpoint-file option. Input-output program-jump option.

e possibly irregular pace at which the external transfer erations are taking place. That is, whenever it is cessary for the internal and external programs to proed precisely in step with each other, the machine can anage to keep the slower-moving external program reast of the high-speed interval program by forcing e latter either to halt or to change its course tempoily. This self-regulation property enables optimum use be made of the concurrent input-output ability of YSEAC on jobs which require considerable transfer of formation into and out of the machine, or which involve earching through voluminous magnetic files.

3. The work program can be interrupted whenever cessary, and a wide variety of special orders can be terpolated into the program either by the operator of the achine or by the external devices. This interruption operty enables the machine to cope with unscheduled b assignments which originate, with little or no advance tice, in external events occurring beyond the supersion of the machine and which must be executed as on as possible for real-time applications such as airaffic control.

It should be noted that these three properties, by eir combined presence, create a fourth property of nsiderable power. That is, acting in concert, they able the machine to be employed effectively as a conl element in a generalized feedback loop.

These over-all properties are derived principally from ree special operating features of the Program Control, e Input-Output Control, and the Manual-Monitor facilies in the DYSEAC, all of which will be described iefly in the following sections.

The term "manual-monitor" has been coined to deribe five types of operations which are either initiated anually by the machine operator, who for example esses a push-button, or else are initiated by the maine itself under conditions which are specified by eans of external switch settings. The former is rred to as a manual operation, and the latter is called monitor operation because the machine must monitor s internal program to determine precisely when the eration should be performed. The type of operation to performed as well as the conditions under which it is be performed are specified by means of external switch ttings.

Manual-monitor operations can readily be specified d initiated by external devices as well as by human erators. Furthermore, since all of the external switch ttings control only dc voltages, the external devices n even be remote from the machine itself, and they can, om a distance (connected to it via ordinary electrical ansmission lines,) exercise supervisory control over e internal program of the machine.

The five types of manual-monitor operations that an be performed are:

1. loading operations, which load new information into specified portions of the machine such as various memory locations and storage registers

2. print-out operations, which print out the contents of these memory locations and storage registers

3. insert-in-the-program operations, in which a new instruction is interpolated into the internal program between the items of the scheduled instruction sequence

4. change-in-the-program operations, in which an entirely new sequence of instructions is substituted for the scheduled instruction sequence

5. halt-the-program orders, with warning signal.

Various combinations of these five types of operations also can be performed. For example, the machine can be told to perform a compound operation such as the following one which involves both loading and insert-in-the-program operations: load the entire memory, and take the next instruction from memory location X. (X represents an arbitrary address number previously entered into the machine via the operator's keyboard or from an input unit.)

Monitor operations are performed by the machine whenever the conditions specified by the external switch settings occur in the course of the program. These conditions can be chosen from among a wide variety of program occurrences, e.g., every time the program refers to a new instruction or makes a reference to the memory; any time the program refers to an instruction to which a special monitor symbol is attached; any time the program refers to a comparison (branch) instruction which results in the selection of either one of the two alternative next instructions; any time the program refers to a location in the memory which matches some specified address number or which falls within certain specified limits; and any combination of these or other special conditions.

By pairing a particular type of manual-monitor operation with a selected set of conditions, a wide variety of special operations can easily be specified and performed. Among the simpler of these are the following examples:

1. Every word written into or read from the memory at each step of the program can be printed out.

2. The contents of a specified memory location can be printed out whenever and as soon as the memory location is referred to in the course of the program, with the option of halting the program at that time if desired. Neither of these operations requires the preparation of any special routine.

3. Various fixed memory addresses or groups of fixed addresses may be continually printed out even while computation is proceeding.

For every manual-monitor operation, the external switches are set to specify not only the type of operation to be performed and the conditions under which it is to be performed, but also the storage places which are to be involved. These storage places can be chosen from a

long list of available locations in the high-speed internal memory and from among five different storage registers in the machine. The memory locations may be designated in a variety of ways: either in the usual way, as an address number, or indirectly as an address specified by the current instruction, or as the address scheduled for next reference in the course of the program. These indirect ways are an advantage to the user of the machine who can, for example, direct the machine to print out the result of each operation without knowing (or being required to specify) the address in which each result is to be found.

Thus, by means of the external switches, certain storage areas within the machine may be utilized by devices remote from it. These remotely located devices can direct that information in certain areas of the memory of the machine be transmitted to them. Similarly, they can arrange to insert new information into various portions of the memory. In this way, at the option of either the external devices or the machine program, or both acting jointly, the DYSEAC can share with these remote devices its high-speed memory and consequently every other part of its internal computing and external storage facilities.

This feature makes it possible for two or more full-scale computers (such as SEAC and DYSEAC) to be harnessed together and work in mutual cooperation on a common task. Each member of such an interconnected group of separate computers is free at any time to initiate and dispatch special control orders to any of its partners in the system. As a consequence, the supervisory control over the common task may initially be loosely distributed throughout the system and then temporarily concentrated in one computer, or even passed rapidly from one machine to the other as the need arises.

Further aspects of the control inter-relationships available in DYSEAC will be discussed subsequently, after the other Special Operating Features in the machine have been described.

Two other special operating features of the DYSEAC are *Breakpoint-File*, which is a program-control operation, and *Program-Jump*, which is an input-output control operation. Before describing these operations, it will be necessary to outline the program-sequencing features of the machine.

The sequence of instructions which specifies the work program for the machine is normally a consecutive one; i.e., consecutively executed instructions are normally located in consecutively numbered address-locations in the memory. Means for interrupting this consecutive sequencing of instructions and for initiating a new sequence are provided by a variety of choice instructions and counter-setting instructions. (See "Comparison" and "File" operations, respectively, in Table 2 which describes all of the instructions available in DYSEAC.) The user of the machine, viz., the programmer, has the facility not only of initiating new instruction sequences at any time but also of choosing between two possible alternative sequences. He may, if he wishes, interleave two distinct sequences, periodically jumping from one to the other in an arbitrary manner. This facility is made possible by a scheme which provides two separate counter-registers for program sequencing, each of which holds an address-number. The address-number in either counter-register may be chosen as the address of the next instruction to be performed.[1]

The address-numbers in these two counter-registers can also be used for another distinctly different purpose, namely, as *base-points*. That is, at the option of the programmer, the address-number in either counter may be used as a base-point, or origin, for those address-numbers in subsequent instructions which the programmer has designated as *relative* addresses. In other words, if address-number X is designated as a relative address in an instruction, the memory location referred to is no longer X but a new location displaced from X by the number stored in the chosen counter. For example, if the chosen counter contains the number C, then whenever address X is designated as a relative address in an instruction, the memory location referred to is $(X + C)$.

In utilizing this counter-register and relative-address facility, the programmer may elect to follow either of two methods. The first method makes use of a *fixed* base-point, which the programmer modifies only occasionally as the program proceeds. The second method makes use of a *floating* base-point, which is the address of the instruction-word itself and therefore progresses constantly. With this second method, the memory locations of the operands referred to in the program may be specified relative to the location of the instruction word even when that location is not known at the time the program is being planned.

The Breakpoint-File operation can now be described. As indicated in Table 2, the control counter-registers can be reset by means of the two types of file operations: File (unconditional) or Breakpoint-File. These two operations allow the programmer to set either control-counter to any arbitrary value, specified either in an absolute manner or relative to its current setting. Since the contents of these counter-registers specify the memory location of the next instruction to be performed, the File operations may readily be used to initiate entirely new branches in the program. Furthermore, since these operations cause a complete record of the status of the program to be written into the memory just prior to starting a new branch in the program, the abandoned branch can be resumed without difficulty later on, if desired.

[1] A.L. Leiner, "Provision for expansion in the SEAC," *Mathematical Tables and Other Aids to Computation*, vol. 5, no. 36, p. 234; October, 1951.

TABLE II

DESCRIPTION OF DYSEAC BASIC OPERATIONS

NAME OF OPERATION	DESCRIPTION OF INSTRUCTION
ddition	Form the sum of the word in alpha and the word in beta, and write the result in address gamma in the memory.
ubtraction	Form the difference of the word in alpha minus the word in beta, and write the result in address gamma in the memory.
ccumulate-and-Overflow-Check	Form the sum of the word in alpha and the word in beta plus the contents of the arithmetic accumulator register. If the sum does not overflow, store the result in the accumulator and proceed to the normal next instruction; if the indicated sum does produce an overflow, however, leave the previous contents of the accumulator unchanged and take the next instruction from address gamma in the memory.
ccumulate-and-Store	Form the difference of the word in alpha minus the word in beta, add the contents of the arithmetic accumulator register to it, and write the sum in address gamma in the memory. Then clear the accumulator.
ummation	Form the sum of the words located in consecutive address locations running from beta through alpha, inclusive, and write the sum in address gamma in the memory.
ultiplication, major, rounded	Form the product of the word in alpha and the word in beta, and write the major part (rounded off) in address gamma in the memory and in the arithmetic accumulator register.
ultiplication, minor	Form the product of the word in alpha and the word in beta, and write the minor part in address gamma in the memory. Also write the major product, unrounded (with proper sign), into the arithmetic accumulator register.
ivision	Form the quotient of the word in beta divided by the word in alpha, and write it in address gamma in the memory. Also write the remainder into the arithmetic accumulator register with the sign of the dividend.
hift	Shift the word in alpha according to the code indicated in the word located in address beta in the memory, and write the result into address gamma in the memory. The seven numerical digits on the extreme right of the word in memory location beta indicate the number of binary places the word is to be shifted and the direction of the shift (left or right.)
Justify	Determine the number N satisfying the following inequalities: $[\beta] \leq [\alpha]\ 2^N < 2\,[\beta]$ Write this number with proper sign into the seven digit positions on the extreme right of the word in address gamma without altering its other digits in any way. Note: $[\beta]$ means absolute value of the word in address beta in the memory, and $[\alpha]$ means absolute value of the word in address alpha in the memory.
Logical transfer	Write in address gamma in the memory those digits of the word in alpha which correspond to one-digits in the word in beta. Leave the word in gamma unchanged in those digit positions which correspond to zero-digits in the word in beta.
Comparison, algebraic	If the word in alpha is algebraically greater than or equal to the word in beta, take the next instruction from the normal consecutive address position. If, however, the word in alpha is less than the word in beta, take the next instruction from address gamma in the memory.
Comparison, absolute	This instruction is similar to algebraic comparison, differing from it only in that the indicated inequalities pertain to the absolute values of the numbers indicated.
File, unconditional	Write the contents of the control counter-registers (and certain other control data) into address beta in the memory; reset specified counter to gamma address-number; adopt contents of specified counter as relative-address base-point in subsequent operations.
Breakpoint-File	This instruction is similar to unconditional File except that it requires the setting of an external Breakpoint-File switch to indicate that its activation is desired. If the switch is not so set, the instruction is passed over without effect.
Input-Output	Load (or print-out) the designated area in the high-speed internal memory from (or to) the designated area in the external storage or input-output unit. After initiating the operation, the program proceeds immediately to the next scheduled instruction. When the external operation is completed, execute program-jump if so indicated.

he Breakpoint-File operation has the same characteristics as the File (unconditional) operation except for ne important additional feature. It requires the setting f an external switch to indicate that Breakpoint-File activation is desired. If this external switch is not so set, the Breakpoint-File instruction is passed over without any effect on the machine. Therefore, by locating Breakpoint-File instructions throughout the program at strategic

points, the course of the program can be changed at these points merely by the turn of a switch. This feature provides a simple and powerful means whereby the course of the internal activities of the machine can be controlled by the external environment.

Before considering the third special operating feature of DYSEAC, namely the *Input-Output Program-Jump* operation, a typical input-output operation in which information is transferred between an external device and the high-speed memory of the machine will be described. It might be noted again that any consecutive areas of the memory in DYSEAC, ranging in size from a single word to the entire memory, can be loaded or printed out even while a program of computation is proceeding. Automatic interlocks are provided to guard against inadvertent attempts to use a memory location for conflicting purposes. For example, if a print-out order is given, the machine is automatically prevented from writing into any memory location affected by the print-out order until the word in that location has been printed out.

A typical input-output operation proceeds in the following manner. First the machine selects the particular external device or unit with which communication is desired. The code number signifying this unit is specified in the input-output instruction. In the second step of the process, the machine runs through a specified number of words or blocks of words on the selected unit, the starting point being the word lying nearest the reading heads for the magnetic wire or tape units, and a fixed origin on the periphery for the magnetic drums. For other types of applications, this step may be used to introduce a variable delay. In the third step of the process, which begins after the requisite number of words has been counted out, the transfer of words between the external unit and the internal high-speed memory takes place. The transfers commence with the numerically smallest address in the indicated block of words and proceed in consecutive order until the numerically highest address is reached, thereby concluding the operation.

Each input-output instruction not only specifies the particular external unit which is involved in the transfer of information and states whether the transfer is to be a Load or a Print-out operation, but also indicates where the information is to be found and to what destination it is to be transferred. Finally, the instruction indicates whether or not a Program-Jump operation is desired after completion of the input-output operation. If a program-jump is desired, then a signal is produced after the input-output operation is completed which causes the program to jump, i.e., the counter-register being used as the source of the next instruction is temporarily abandoned, and the instruction word in the address location specified by the other counter-register is executed in its stead.

This program-jumping feature is useful in many situations. For most applications which make use of concurrent loading or printing-out of the high-speed memory while computations are proceeding, the precise length of time required to complete the external operation is either indeterminate or else quite difficult to predict. A typical example of an instance of this type occurs when it is necessary to hunt for a particular word or group of words in an unknown location on a long magnetic tape reel, where a word can be identified as one of the desired type only after it has been read into the machine and subjected to an analysis of its characteristics. Since efficiency requires that information be read into the high-speed memory in fairly large blocks, it is desirable during the comparatively slow procedure of reading in the information to make use of the ability of the system to proceed concurrently on other independent phases of the program. By means of the input-output program-jumping feature, the programmer is able to direct that these other independent phases of the program be allowed to proceed uninterrupted until the specified loading of the information is completed and that as soon as the loading is completed, the program should jump to an alternative specified routine which is designed to analyze the newly received information and to decide whether or not to retain it or to continue hunting on the tape.

An analogous need arises when it is desired to check the accuracy of information printed out on the external medium by reading the information back into the machine and comparing it with its original source. A process of this sort would require a Print instruction followed by a Load instruction. In order to avoid having the program stand by while the print-out operation is being completed, the programmer can arrange for other internal operations to be carried out concurrently which would be interrupted only when the print-out operation is concluded, at which time the Load instruction would be initiated.

More generally, the Program-Jump facility provides a means by which the machine can order an external unit to carry out an assigned task and at the same time periodically report back its progress in carrying out the task so that the machine can maintain the closest possible check on the external operation and redirect it properly as the need arises.

After effecting a program-jump, the new program that is initiated may, as soon as its final instruction is performed, cause the machine to resume the interrupted program where it left off, if the programmer so desires. An automatic interlock relieves the programmer of the burden of having to estimate precisely how long a time will be required for the original input-output operation to be completed and insures that all the steps in the program will be carried out in their proper sequences. The system is so designed that the order which appears first in the program must be satisfied before any subsequent conflicting order can be carried out.

In concluding the discussion of the special operating features of DYSEAC, it should be noted that the various interruption facilities which have been described are

ased on mutual cooperation between the machine and e external devices subsidiary to it, and do not reflect erely a simple master-slave relationship. With the reakpoint-File feature for example, the external device hich operates the Breakpoint-File switch initiates the quest for the branching action, but the actual execution the operation must await confirmation of the request by e machine, i.e., the occurrence of a Breakpoint-File instruction in its program. In the case of the Input-Output rogram-Jump, on the other hand, the initiation of the quest originates in the internal program (via an Input-utput instruction containing a jump-order symbol,) while e actual execution does not take place until the external device returns the proper signal, signifying termination of the operation. The third variety of internal-xternal action, the manual-monitor type, exhibits spects of both types of control relationships. For the mple manual operations, the external unit (or the perator) exercises full control over both the initiation nd execution of the request, e.g., by pushbutton. For e monitor operations, however, the request can be considered as initiated externally (by turning breakpoint-hoice switches) but the actual execution of the operation does not occur until the requested conditions arise the course of the internal program.

These varied internal-external joint-control relationships are summarized in Table 3. For each of the special erating features (Breakpoint-File, Program-Jump, and anual-Monitor operations,) Table 3 indicates whether an ternal or external source initiates the request for the eration and whether an internal or external source decides to execute the operation. This same information is

TABLE III

TERNAL-EXTERNAL JOINT-CONTROL PROPERTIES OF DYSEAC SPECIAL FEAUTERS

SPECIAL OPERATION	Source Which Describes Operation	Source Which Initiates Operation	Source Which Decides to Execute Operation
eakpoint-File peration	Internal	External	Internal
ut-Output rogram-Jump eature	Internal	Internal	External
nual operation	External	External	External
nitor operation	External	External	Internal
ONVENTIONAL OPERATION			
w instruction rought in from in-ut unit by program	External	Internal	Internal

so given for the more conventional method of control, hich consists of calling new instruction words into the mory of the machine by means of a programmed input struction. It is evident that the control inter-relationships provided by the special features of DYSEAC are distinctly different for each special operation and that equivalent control versatility cannot be achieved by the more conventional program method. Indeed, the foregoing special features were incorporated into DYSEAC only because the joint-control properties needed for its intended applications could not be secured satisfactorily otherwise, even by the use of special or complex internal programming procedures.

OVER-ALL FUNCTIONAL ORGANIZATION

The over-all functional organization of the DYSEAC is indicated in the block diagram of Fig. 1, which shows the major communication routes and control relationships in the system.

The High-Speed Memory shown in the center receives and distributes to the other units the information (numerical and instruction) to which the most rapid access is needed for carrying out the work-program of the machine. The memory communicates principally with five major units of the system. Of these, two are concerned primarily with internal processing affairs and three with external relations. A continuous flow of digital information may be maintained simultaneously between the memory and the inward-looking and outward-looking types of units. The latter types, which serve to communicate with the external devices represented on the left side of the block diagram, include the *Input-Output Buffer*, the *External Selector*, the *Concurrent Input-Output Control*, the *Display Staticizer* and the *Serializer*.

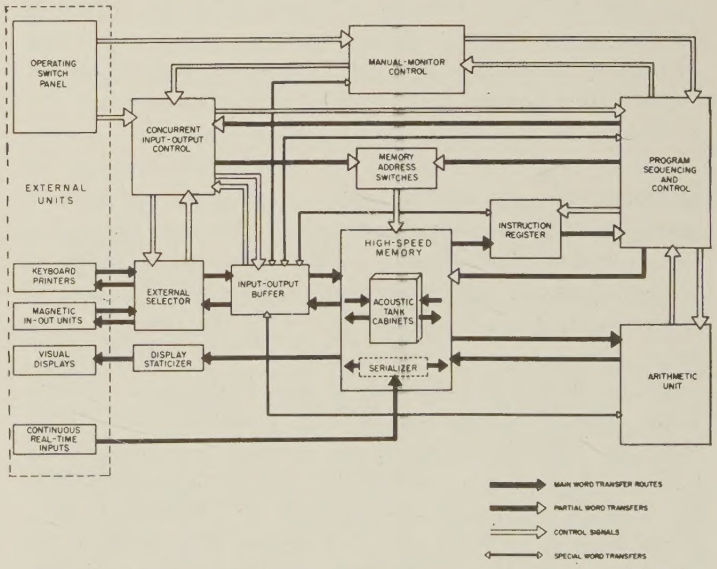

Fig. 1 – Over-all functional organization of the DYSEAC system.

The function of the Input-Output Buffer is to transmit information at the proper repetition rates from the external unit to the internal memory during an input operation, and in the reverse direction during an output operation. The buffer receives words from the memory at

the normal one-megacycle internal repetition rate and then transmits them out digit-wise at the proper measured rate appropriate to the external unit. The external unit itself (via the External Selector) specifies the word format and repetition rate appropriate to it. Provision is made in the Input-Output Buffer for handling information in various forms, e.g., in a single-channel serial form for magnetic wire units, in serial-parallel 4-channel form for magnetic tape units or Flexowriter, and in fully parallel 45-channel form for magnetic drum. A wide variety of other formats is also available if needed. The initial range of repetition rate may be up to 16 kilocycles (single channel.) If higher rates are desired in the future, an additional buffer storage register may be added to the system.

The External Selector is a high-speed electronic switching device which selects the external unit with which an input-output operation is to be performed. It provides the signal required to operate the proper multichannel electromechanical relay or other device which completes the circuit connections for the lines carrying both the digital information and the control signals needed to operate the external unit. The design of the External Selector has been chosen so as to be readily expandable whenever additional external units become available. The initial model contains provision for selecting among up to 48 distinct external mechanical relay switches, but it can be expanded, with about an equal amount of additional equipment, to be capable of handling up to 256 distinct information channels, such as individual parallel magnetic-drum channels or high-capacity magnetic filing systems.

The External Selector accomplishes its switching function by a process of scanning successive switching channels in synchronism with a counter located in the Input-Output Control Unit, starting from a fixed origin. As a result, a gradation of electronic switching access times is available, ranging from a minimum of about 25 microseconds, for the channel closest to the origin to a maximum of about six milliseconds for the last channel of an expanded 256-channel model. This wide range of switching speed can be matched to the operating rates of the external devices themselves, e.g., the first 20 channels, whose average access time is 0.25 milliseconds, might be chosen to communicate with high-speed external units capable of reacting in 1 to 2 milliseconds, while the last 200 channels, whose average access time is about 4 milliseconds, switch with speeds compatible with the average rotational access time of a 3,600-rpm magnetic drum. A feedback checking feature is provided in the External Selector for insuring that one and only one channel is selected and that it is the channel requested by the Input-Output Control Unit.

The Concurrent Input-Output Control has the function of regulating the detailed progress of all input-output operations requested in the course of the internal program. It directs the flow of traffic between the memory and the Input-Output Buffer, and between the Input-Output Buffer and the External Selector. It instructs the External Selector to step along to the proper switch channel, checks that contact is made with the desired unit, and signals the Input-Output Buffer to proceed to accept digits either from the external unit during an input operation or from the high-speed memory during an output operation. It receives signals from the Input-Output Buffer as each complete word is transferred, and it not only keeps count of the total number of words handled, but also keeps track of which address in the high-speed memory contains the word currently to be transferred. This information is transmitted to the Memory Address Switches at the proper time.

In the comparatively unlikely event that both the Input-Output Buffer and some internal unit should simultaneously demand access to the high-speed memory, the Concurrent Input-Output Control resolves the conflict by according temporary priority to the external operation.[2] Likewise, it referees conflicts or inconsistencies between the internal program and the progress of external operations. It also notifies the Program Control unit at the termination of an input-output operation so that the program-jump may take place. Its other functions include regulation of the memory error-seeking scan process and the Summation operation.

The Display Staticizer and the Serializer are input and output organs adapted especially for real-time operations. The Display Staticizer is a register storing 28 bits statically in parallel for controlling, for example, a digital-to-analog converter that provides deflection voltages for crt visual displays. The register is loaded periodically, cycling through a chosen group of words in the high-speed memory. The size of this group (one to 32 words) and its location in the memory are adjustable manually. The cycling proceeds through the specified area independent of the internal program and in no way interferes with the use of the area by any other units, such as Arithmetic Unit or Input-Output Buffer.

The Serializer unit is provided for continuous real-time external input devices. This unit can accept one full word of 45 bits delivered in parallel in the form of asynchronous pulses from an external unit (minimum pulse duration about 50 microseconds) and can transmit the word in synchronized normal serial form to any other units of the system capable of reading words out of the high-speed memory. The Serializer, however, can provide words to the other units at about 4½ times the average access rate of the acoustic memory.

[2] A.L. Leiner, "Buffering Between Input-Output and the Computer, Review of Input and Output Equipment Used in Computing Systems," *Joint AIEE-IRE-ACM Computer Conference*, s-53, pp. 28-30, March, 1953.

The Arithmetic Unit (lower right-hand corner of Fig. 1) rries out a group of 13 arithmetic or choice operations. ithmetic results are written directly into the high-eed memory, and control signals specifying the out-me of the discrimination operations are sent directly the Program-Sequencing and Control Unit where they rve to modify the choice of memory location from which e next instruction is to be read. A third route of mmunication to the Input-Output Buffer, labelled special word transfers", represents the facility of ading or printing out the contents of the arithmetic cumulator register directly via the Flexowriter or agnetic input-output units.

The remaining unit in direct communication with the gh-speed memory is the Instruction Register. Instruc-on words are transferred one at a time, as needed, from e memory into the Instruction Register. From this unit, eces of information contained in different segments of e instruction word pattern are selected by the Program ntrol Unit and transmitted to various other internal its throughout the system. From the Program Control nit, digital address codes pertaining to each phase of ch operation are sent to the Memory Address Switches order to make the specified memory locations avail-le to the Arithmetic Unit and Instruction Register at e proper time. This information is made available to e Concurrent Input-Output Control at the same time, for ecking against possible conflict with current input-tput operations. Furthermore, whenever an input-output struction is received in the Instruction Register, the rogram Control routes it immediately to the Input-Output ntrol Unit and proceeds to call a new instruction word t of the high-speed memory. Finally, during the File-pe operations, various items of program-control informa-on can be written out of the Program-Control Units rectly into the memory. This same information can also transferred into or out of the system via the external put-output units over the indicated special-word-transfer th to the Input-Output Buffer.

The last major unit to be noted is the Manual-Monitor ntrol. This unit is responsible for regulating and nchronizing the carrying out of joint internal-external erations. Its major functions are:

1. to interpret the breakpoint conditions received m the external Operating Switch Panel,
2. to observe the progress of the internal program d recognize when the specified breakpoint conditions ise, and
3. to deliver signals temporarily halting the internal ogram, if necessary, setting up the required special-ord-transfer routes, and initiating the specified inter-lated internal or external operation.

The proportion of physical space required by the quipment for carrying out the joint internal-external ntrol operations of DYSEAC is indicated graphically in Fig. 2. The areas marked off on this chart have been made directly proportional to the number of physical packages required for realizing the various functional units just described, exclusive of the memory. It can be seen that the equipment for performing Manual-Monitor operations, Breakpoint-File operations, and Input-Output address-conflict and program-jump operations (shaded

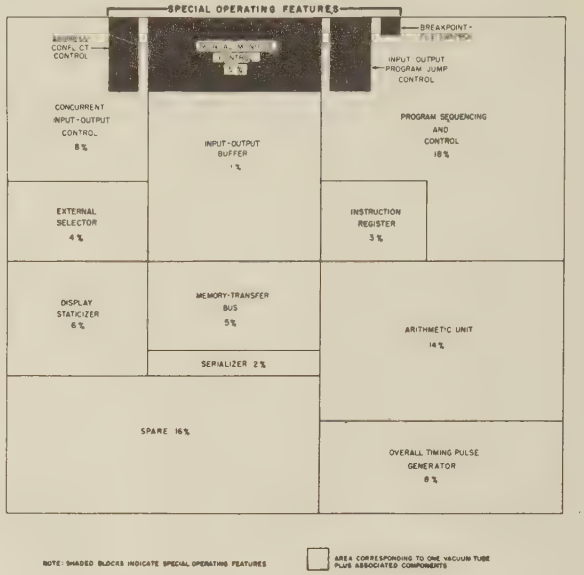

Fig. 2 — Proportion of space required for DYSEAC special operating features.

areas on the chart) constitute only about six per cent of this total. Also, about sixteen per cent of the total physical space available, labelled "spare" on the chart, has been left unused and can be utilized for annexation of other internal computing or control units if so desired.

OPERATING CAPABILITIES

As a result of its special features, the DYSEAC possesses three versatile operating properties which may be summarized as follows:

1. The external devices harnessed to the machine can gain access at any time to all or to any part of the internal memory without disrupting the internal computing program. Moreover, practically continuous input-output access to certain special parts of the internal memory is available for the use of specialized external units needing faster-than-average access, e.g., units which provide continuous visual displays for the operator or which produce certain manual or automatic control signals for the computer.

2. The DYSEAC can operate with a wide variety of input-output devices ranging from electromechanical typewriters through magnetic storage devices to analog-digital converters associated with different types of sensing devices and servomechanisms. Some of these devices deal with detailed digitalized data at magnetic

recording rates. For these, the system contains facilities for accepting and transmitting data at a variety of repetition rates and word formats.

3. Whenever necessary, the progress of the internal program can be regulated, scaled, and synchronized by events occurring beyond the supervision of the machine.

Because of this ability of the machine to turn its attention to any of its wide family of subsidiary devices and to interrupt or redirect its over-all program in order to assist or manage them, DYSEAC can be used for investigating many diverse areas of potential application ranging from the simulation and control of links in a data-communication network to the high-speed processing of business data.

As an example of a potential application which requires such capabilities, consider an installation engaged in the automatic processing of business accounts and records. In an application of this sort the main task of the computer might be the routine processing of monthly accounts. The data to be processed would be withdrawn automatically by the machine from the external magnetically recorded files,[3] would then be properly combined with newer data, and finally the up-to-date information would be returned to the files. Even while these operations are progressing automatically, however, the contents of the files would need to be available to the clerical staff of the office for inserting occasional corrections or revisions of data, or for answering scattered spot requests for information. Moreover, in some case, the computing services of the machine would be needed for carrying out special minor processing tasks on the data being withdrawn from the files in this manner. At the same time, batteries of printers might be systematically going through the files and routinely printing out those portions for which the monthly processing was already complete. Similarly, the routine entry of new data, such as sales records, into the portions of the files not yet reached for processing might be going on.

Obviously, it would be highly desirable to be able to carry out any of these several operations at will, with as little disruption as possible either to each other or to the main task. Because of the unforeseeability of some of the operations (such as the spot requests for information) or the uncertain or variable operating rates of some of the external devices (such as mechanical printers) although the *nature* of the functions may be prearranged and suitable instructions may be prepared and inserted into the machine in advance, the exact *time* for their actual initiation or the *sequence* of their execution can not in any way be precisely scheduled in advance. In order to operate efficiently, therefore, the machine should be able *on a completely unscheduled and intermittent basis* to share both its program-control and its internal storage facilities with its external subsidiary devices and human operators.

As a second example of a potential application which requires these capabilities, consider an installation engaged in the control of air traffic at an airport terminal. For this application, the human operator can be coupled to the machine system:

1. through the medium of a visual display device which exhibits graphically the numerical data stored inside the internal memory, and

2. by means of a battery of manual control switches capable of inserting new numerical data or certain new control commands into the machine. The numerical data displayed by the machine represent in real time a map of the predicted traffic patterns in the neighborhood of an airport, e.g., the predicted locations, based on latest scheduling information, of all aircraft inside a certain area. The human operator can, by means of the manual input-controls, enter newer data into the machine as the information becomes available, interrogate the machine for more detailed information concerning certain individual flights as the need arises, and instruct the machine to exhibit the effect to be expected from issuing revised flight-control orders. In the latter case, parts of the internal information of the machine must be presented to the operator in a rather complex pictorial form in order to be meaningful to him. Applications of this sort, like the previous one, require a constant interchange of intelligence between the computer and its operator, and between the computer and other devices.

A third type of potential application involves the utilization of automatic computers for the control of automatic machinery: a first step toward the so-called automatic factory. Here, the main tasks of the computer involve: first, storing the prearranged procedure or series of steps that are to be taken by the automatic machinery which is carrying out the manufacturing process; second sensing the progress of the machines or the results of their activity on the product being produced; third, after a complex analysis or comparison of the desired end result with the observed result, determining the appropriate next step to be taken; and finally, issuing appropriate signals which will tend to guide the external tools or regulators in a preferred direction. In the latter case, the computer not only is performing many of the functions already described but also is acting as an element in a feed-back control loop.

Since the DYSEAC has all of these control capabilities, it can be a highly effective tool for exploring any of these diverse areas of potential application. A particular area will naturally require the annexation of terminal devices specific to the nature of the task; yet there need be little or no alteration in DYSEAC itself to do this. A complex inventory-control application will be one of the first areas to be explored with this new system.

[3] S.N. Alexander, "Summary and Forecast," op. cit., pp. 137-139.

A TIME-SHARING ANALOG MULTIPLIER

H. Freeman and E. Parsons
Sperry Gyroscope Company
Great Neck, N.Y.

SUMMARY—This article describes the design of a high eed electronic analog computing circuit which easily lends self to time-sharing applications. By making use of a special gh accuracy electronic switch and circuitry carefully degned to be independent of tube characteristics, it was posble to achieve a full-scale accuracy of better than 0.2 per nt over a wide range of input values. The unit described was ilt to carry out 400 complete multiplications and divisions one second.

INTRODUCTION

Several years ago work was undertaken by the thors on the development of a high speed multiplying d dividing circuit. The purpose of the investigation as to determine whether or not a satisfactory electronic nalogue computing circuit could be obtained for high eed time-sharing. The principle on which the multiplyg and dividing circuit was based has already been scribed in the literature by others.[1] The work that was rried out was concerned only with obtaining an experiental model which could be used to evaluate the capalities of the multiplier with respect to speed of operon, accuracy, complexity and reliability.

PRINCIPLE OF OPERATION

The following is a brief description of the principle which the multiplier is based. Two voltages "sweep" om zero to some maximum value. The sweeps are idental in form (i.e., both linear both exponential, or both nusoidal, etc.,) The amplitudes of the sweeps are fferent and taken as two of the inputs. A third input oltage is compared to one of the sweeping voltages in ch a way that when the sweep voltage is equal to it, e other sweep voltage is sampled. The value of the tter sweep voltage at this instant will be proportional the product of the amplitudes of two of the inputs vided by the third. This is illustrated in Fig. 1.

If the two input voltages, $\bar{E}_a$ and E_c, are suddenly plied to two identical linear networks whose output sponse with time is then $E_aN(t)$ and $E_cN(t)$, and if $E_cN(t)$ is compared to a third input voltage, $\bar{E}_b$, then if $E_aN(t)$ is observed at the instant at which $E_cN(t)$ equals E_b, the value of $E_aN(t)$ will be

$$\frac{E_a \cdot E_b}{E_c}.$$

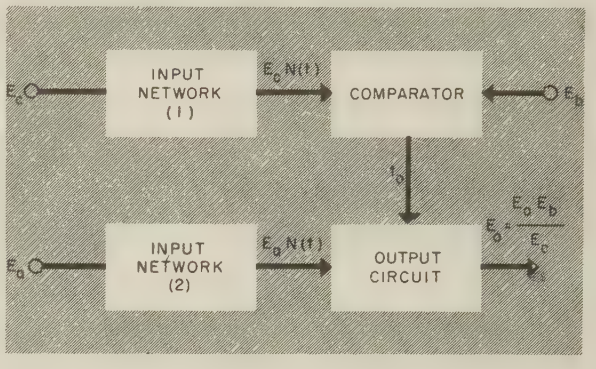

Fig. 1 — Diagram of sweep voltage sampling.

The expression for $N(t)$ is not important. For instance $N(t)$ might be given by $\sin\omega t$, by $e^{-\alpha t}$, or by $1 - e^{-\alpha t}$, etc.

As soon as one of the sweep voltages is equal to the comparing voltage, the answer to the problem is available as a voltage stored on a capacitor. The higher the sweep speed which is used, the less will be the time required to obtain a solution. Accuracy consideration will place an upper limit on the sweep speed. As soon as one solution is obtained, a new set of inputs may be applied and a new problem solved. Thus, the multiplier can rapidly accept a large number of problems, each very much different from any other, and is, therefore, ideally suited to time-sharing techniques.

The basic units of the multiplier consists of two input networks, a comparator and an output circuit. The input networks are used to generate the desired sweeps, the comparator determines the instant at which one of the sweeps is equal to the fixed input, and the output circuit "reads" the other sweep at this same instant.

Statically, the multiplier has no theoretical error; i.e., it does not make use of any approximations except in a practical sense. However, if any of the inputs are changing during the multiplication cycle, a dynamic error is introduced which is roughly proportional to the frequency of this change. For very rapidly changing inputs, the errors would be quite large. The multiplier is not

ohn Broomall and Leon Riebman, "A Sampling analogue omputer, *Proc. I.R.E.* vol. 40, pp. 568-572; May 1952.

suited for signals whose frequency is appreciable compared to the operating frequency.

Any change of the inputs occurring before or after the sweep operation has no effect on the output. Thus, for time-sharing, the inputs can be changed during "deadtime", and after the change is completed, the sweeps can again be initiated. The next change of inputs must then await completion of the sweeps and the comparator action. Thus, a multiplier having an operating frequency of 1000 cycles per second can accept as many as 1000 different sets of inputs and obtain 1000 corresponding outputs without any theoretical error whatsoever.

The main advantage of this method of multiplication is the fact that no settling-time is involved. The solution of the problem is available (as a voltage stored on a capacitor) at the instant at which the comparator notes equality between one of the sweeps and the fixed input. In this respect the multiplier differs markedly from multiplying circuits in which the output is obtained as the area under a pulse.[2,3] Such multipliers require low-pass filtering over several cycles to obtain a voltage proportional to the desired product. For sudden changes of the input data (as would occur in time-sharing applications), these multipliers have a definite transient response time so that the desired output is not available until the steady-state condition is reached. It is the absence of any settling-time which makes the multiplier described here so useful for time-sharing applications.

The accuracy of the multiplier depends primarily on the proper initiation of the sweeps, the identity of the two sweep networks, the sensitivity of the comparator and the fast "reading" action of the output circuit.

As the frequency is increased the time error of the comparator and output circuit may become an appreciable part of the operating cycle. This time error is the difference in time between the instant at which the sweep voltage exactly equals the fixed voltage and the instant at which the other sweep voltage is "read." If this delay is one microsecond, it is only one part in a thousand for an operating frequency of 1000 cycles per second. However, it is one part in 100 for an operating frequency of 10,000 cycles per second.

CIRCUIT DESIGN

In designing the actual circuits for the multiplier, care was taken to eliminate the effects of tube characteristics. Since the multiplier depends in its operation on the charging and discharging of certain capacitors a very liberal amount of time was allowed for these charging or discharging actions to take place. All components and circuits were designed for an accuracy of 0.05% per cent. Thus, a capacitor which was intended to be discharged prior to the start of another operation was given a discharge time-constant which would permit it to discharge to 0.05 per cent or less in the allowed time. This principle was followed throughout the entire circuit design.

It was apparent at the outset that a high-speed and high accuracy electronic switch would be necessary. A switch that would meet these requirements was specially developed. It consists essentially of a dc amplifier followed by a series gate tube with a large amount of feedback around the combination.

By following these general precepts in the design, a circuit was obtained which was entirely devoid of any critical elements. In not a single case was the individual performance of a vacuum tube relied upon to contribute to the circuit performance. In this way it was possible to obtain a circuit which would not require any balancing and was completely insensitive to tube changes. An exception to this exists in the dc amplifiers that were used. Although drift stabilized amplifiers were available, they were not incorporated into the experimental model. The final circuit contained 21 vacuum tubes of which approximately five could be eliminated in a future design. Since the multiplier circuit was strictly of the breadboard type, no special effort was made to keep the number of these tubes to a minimum.

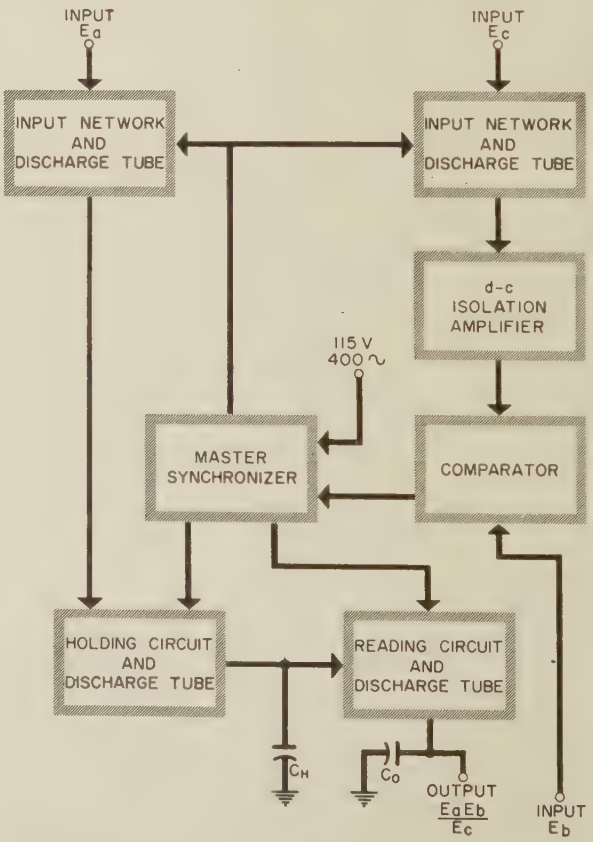

Fig. 2 – Block diagram shows circuit design.

[2] "Electronic Instruments," M.I.T. Radiation Laboratory Series, vol. 21; pp. 50-53.

[3] C.D. Morrill and R.V. Baum, "Stabilized time-division multiplier," *Electronics*, vol. 25; no. 12, pp. 139-141; December 1952.

The block diagram for the experimental model of the ultiplier is shown in Fig. 2.

A unit called the master synchronizer controls the me sequence required for the multiplication process. his time sequence is shown in Fig. 3. At time t_1 a pulse

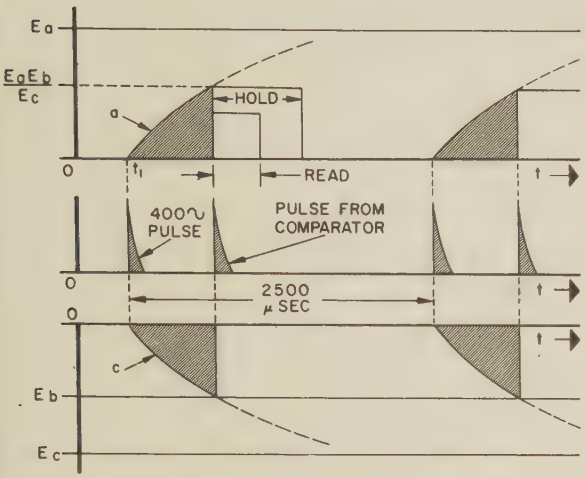

Fig. 3 — Time sequence in multiplication process.

roduced by the 400 cps synchronizing signal initiates he sweeps determined by the input networks and the oltages E_a and E_c. At the instant the sweep "c" beomes equal to E_b (determined by the comparator) the nput networks are immediately discharged. During the weep time the holding circuit charges the capacitor C_H o the instantaneous value of the sweep "a". When the nput networks are discharged, the holding circuit beomes non-conducting and the capacitor C_H retains the aximum voltage level that the sweep had reached. The eading circuit then transfers the voltage stored on C_H o the output capacitor C_o. Following this the holding apacitor C_H is discharged in preparation for the next ultiplication cycle while the capacitor C_o retains the esired output voltage.

The use of both a holding circuit and a reading ircuit contributed two important factors to the accuracy btained. First, since the capacitor C_H was not required o retain the output voltage it could be discharged prior o each multiplication cycle. Therefore, instead of having o obtain its charge only at the instant the sweep "c" ecomes equal to E_b, the capacitor must merely follow he input sweep. Second, since the desired voltage is eld by C_H, the sampling time available for the output apacitor to take on its charge can be relatively long. ince the rate of change of the input should be small ompared to the repetition frequency of the multiplier, the hange in charge required by the output capacitor will be mall. Therefore accurate transfer of the voltage being eld by C_H is easily obtained in the time allowed for eading.

INPUT NETWORKS AND DISCHARGE TUBES

The input networks (Fig. 4) were chosen as series resistance-capacitance combinations, the voltage across the capacitance giving the desired sweep characteristics.

When the multiplication process is to begin, the the grids of the discharge tubes are made highly negative. This allows the capacitors to charge, producing a sweep of the form

$$V_o(t) - VK \qquad 1 - e^{-\alpha t}$$

where K and α are constants determined by the input network and the input impedance of either the holding circuit or the isolation amplifier. Since similarity of the two sweeps is essential for accuracy, the cut-off state of the triodes is used to initiate the sweeps. This assures that any differences between the two tubes will have no effect.

Because a repetition frequency of 400 cycles per second was used, a maximum of 2500 microseconds was available for one complete multiplication cycle. To allow adequate time for "reading," 1500 microseconds was arbitrarily fixed as the maximum sweep time. The time constants for the input networks were then chosen so that the output, as determined by the above equation, would rise to approximately half the input value when a maximum sweep time was used. Therefore, only the relatively steep portion of the sweep was ever used for comparison.

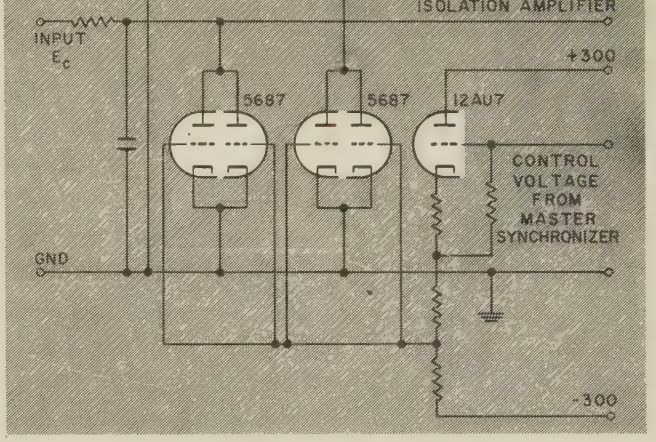

Fig. 4 — Input networks and discharge tubes.

When the comparator acts, the discharge tubes are made highly conducting allowing the capacitors to discharge. The time available for discharge is always at least 1000 microseconds. The small discharge time constant insures that the capacitors will be discharged to a voltage less than 0.05 per cent of the maximum voltage ever stored on them.

Since one of the important factors determining accuracy is the similarity of the input networks, the elements in the two circuits were matched to 0.05 per cent.

COMPARATOR

The accuracy of the multiplier depends in part on the ability of the unit to "hold" the value of the sweep voltage at a prescribed instant of time. Hence, it is necessary to produce a very sharp pulse the moment the sweep "c" becomes equal to E_b. The "multiar" type of comparator shown in Fig. 5 was used.

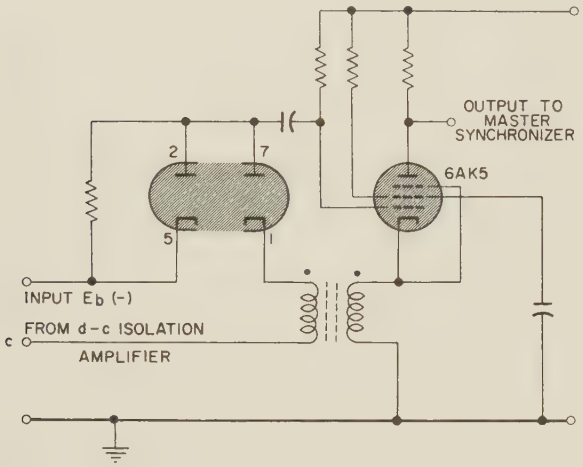

Fig. 5 – Comparator is "multiar" type.

This particular type of comparator requires the use of negative inputs. At the instant the sweep "c" becomes equal to E_b, the regenerative action through the pulse transformer produces a sharp rise at the plate of the pentode.

The function of the diode (2-5) is to compensate for any drift in the diode (7-1) due to aging or filament temperature variations.

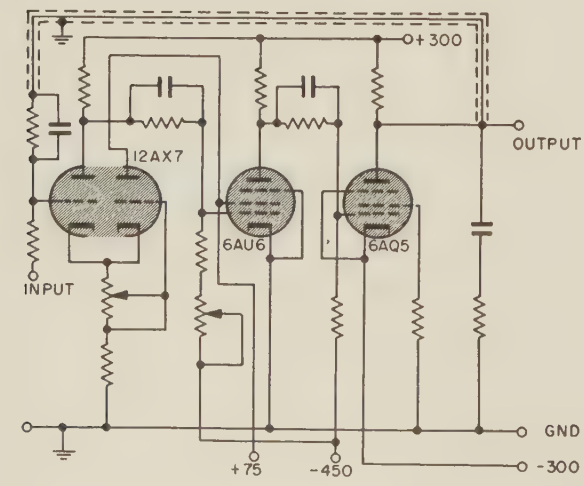

Fig. 6 – The dc isolation amplifier circuit.

DC ISOLATION AMPLIFIER

As stated in the preceding section, the input to the comparator requires that "c" be a negatively sweeping voltage. Since the input networks produce a positively sweeping voltage, the dc isolation amplifier shown in Fig. 6 is used to produce the necessary 180 degrees phase shift. By adjusting the voltage divider in the grid circuit of the 6AU6, zero output for zero input can be obtained.

HOLDING CIRCUIT

The holding circuit is shown in Fig. 7. The capacitor C_H connected to the output of the series gate tube retains the maximum value of the input voltage. The small charging time required for accurate following of the input voltage is provided by the feedback of the amplifier. Gating is provided by means of a twin triode, one side of which is connected as a diode. The tube is located beyond the last stage of dc amplification but included in the feedback loop of the amplifier. It can be seen from Fig. 7 that a positively increasing voltage at the input will be transmitted through the diode to the capacitor C_H as a negatively increasing voltage. When the input is removed the capacitor will retain its charge as long as the triode gate is non-conducting.

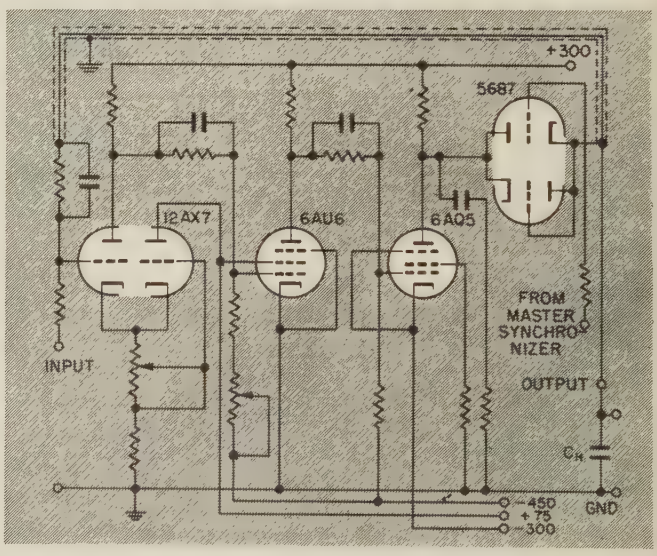

Fig. 7 – Holding circuit used in multiplier.

Because of the feedback action of the amplifier, the capacitor discharges very rapidly when the triode is made conducting. Since the cathode of the triode is connected to the capacitor, the grid voltage swing necessary to make this tube conducting or non-conducting must exceed the range of the voltages which may be stored on this capacitor.

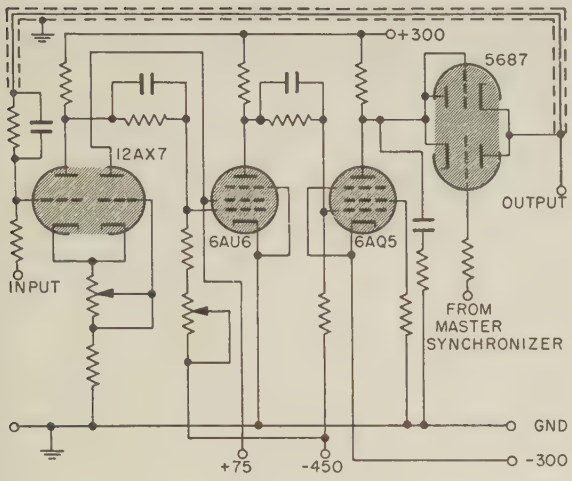

Fig. 8 – Reading circuit used in multiplier.

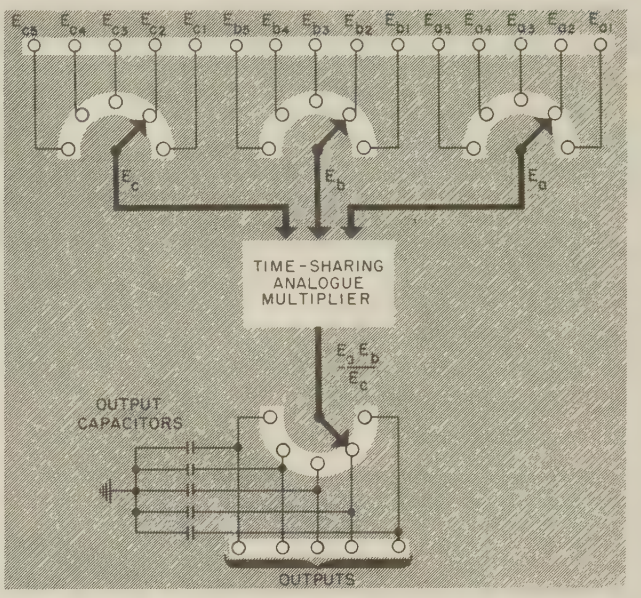

Fig. 9 – Multiplier circuit arranged for time-sharing among five separate data channels.

READING CIRCUIT

The reading circuit shown in Fig. 8 is essentially same as the holding circuit. The only difference being that since the input is now negatively increasing voltage, the gating circuit connections are reversed.

It should be noted that the cathode of the gate triode is now connected to the plate of the last stage of dc

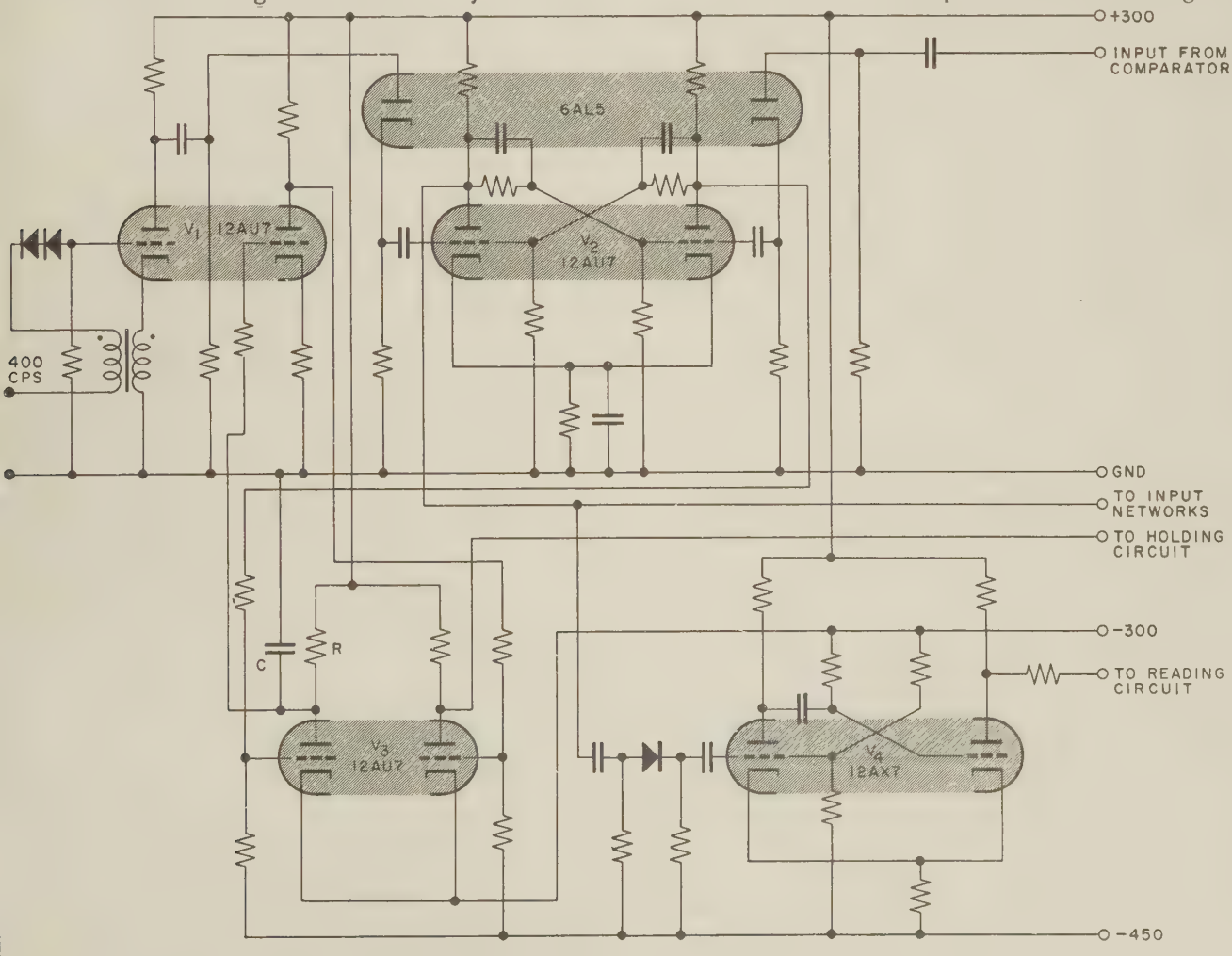

Fig. 10 – Master synchronizer circuit is designed to control timing sequence of various units.

amplification. Hence the voltage swing on the grid of the gate triode must be large enough to overcome the effect of the cathode swing.

Because of the direction of the gate diode in this circuit, the output capacitor voltage will be increased as soon as the sweep voltage rises above the voltage stored on the capacitor. If the maximum value of the input is less than the stored voltage, the capacitor will be discharged to this new value during the reading sampling time. In any case the charge will be small and accurate storage of the desired voltage will be obtained in the ample time allotted for "reading." Because of the high power, low impedance charging of the reading-circuit, the output capacitor may be of large value, insuring that it will retain the output voltage accurately for a long time. Time-sharing for a large number of channels is now made possible since it may be sufficient to recompute each channel only once a second without having the output voltage drop by more than 0.05 per cent when the capacitor is connected to a one megohm resistor.

When the multiplier is time-shared, the output selecting switch is interposed between the reading circuit and the capacitor C_o (see Fig. 2.) A separate storage capacitor is required for each channel. Fig. 9 shows the circuit set-up for time-sharing among five separate problems. Individual output storage capacitors are provided so that the outputs are continuously available. The time sharing switches may be either mechanical or electronic. If they are electronic, switch circuits of the holding or reading circuit type (but with both triodes gated now) are required both at the inputs and output of the multiplier.

MASTER SYNCHRONIZER

The circuit designed to control the timing sequence of the various units is shown in Fig. 10.

Excitation of the first half of V_1 by the 400 cps signal produces a square wave which is differentiated and the negative pulses clipped. A positive pulse at the grid of the left half of the bistable multi-vibrator (V_2) produces a decreasing voltage at the corresponding plate. This places a highly negative voltage on the grids of the discharge tubes of Fig. 4, allowing the capacitors to start "sweeping."

The rise of the right plate of V_2 makes the left half of V_3 conducting. As a result this plate drops to a low value, cutting off the second half of V_1. The right half of V_3 is then made conducting, causing the large negative voltage from its plate to be applied to the holding circuit gate tube which now becomes non-conducting.

When the pulse from the comparator triggers the right side of the bistable multivibrator (V_2), the multivibrator changes its stage, applying a positive voltage to the input network discharge tubes (where the sweep capacitors are then abruptly discharged). The fall of the right half of V_2 makes the left side of V_3 non-conducting. Because of the *R-C* time constant, there is a delay before the plate voltage of V_3 rises to a point where the right half of V_1 can again conduct. This delay is the "holding" time, during which the voltage stored on C_H is transferred to C_o by the reading circuit.

The reading circuit gate is also made conducting when the comparator pulse resets the bistable multivibrator. The delay multivibrator (V_4) controls the "reading-time," which must, of course, be less than the "holding-time" (see Fig. 3.)

All the above action takes place before the next pulse from the 400 cps source occurs, at which time the entire cycle is repeated.

CONCLUSION

Tests on the breadboard model of the multiplier showed a full-scale accuracy of better than 0.2 per cent over the range of input values shown in Fig. 11. The shaded area represents the region of operation for

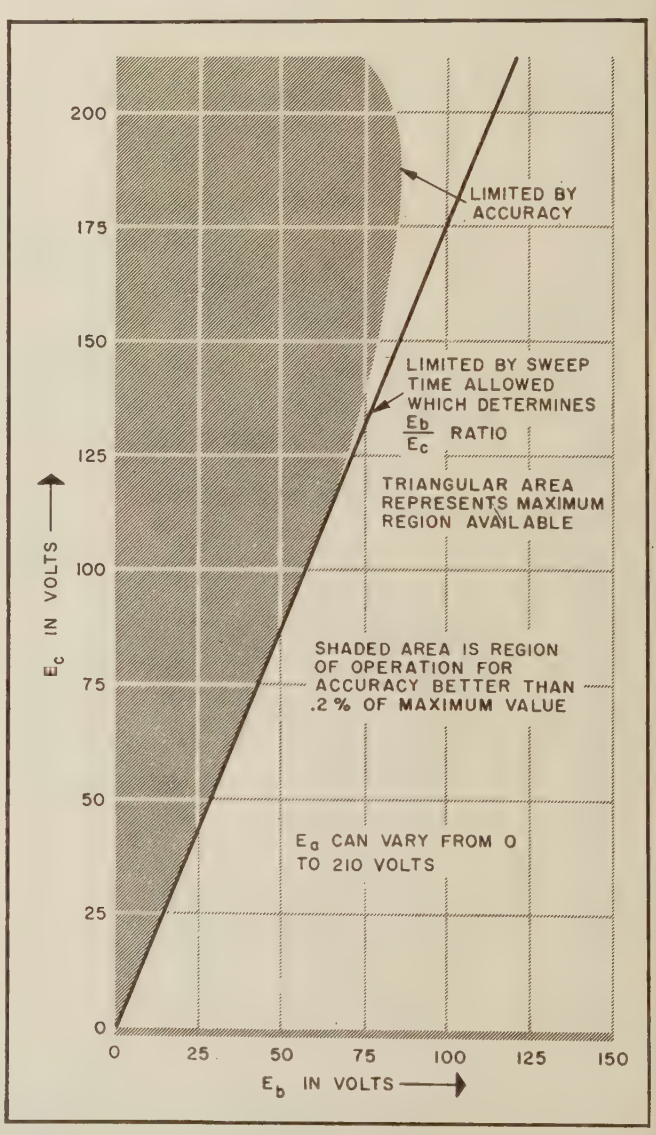

Fig. 11 — Accuracy and range graph developed from tests on breadboard model of multiplier.

curacies of at least 0.2 per cent. If a point determined the value of E_b and E_c lies within the shaded area, a may assume any value from 0 to 210 volts (the limit linearity of the dc amplifiers.) Limitations of the sting equipment available did not permit establishing e actual limit of accuracy though indications are that e multiplier is actually accurate to better than 0.1 per nt.

As described here the multiplier is a single quadrant vice; that is, the input quantities cannot change in larity. The experimental model required two positive and one negative input. The negative input restriction was imposed by the type of comparator used. These polarity restrictions are strictly a circuital rather than a functional limitation.

Indications are that greater accuracy is possible with only minor improvements in the circuit described in this paper. Also, because of the positive action of the multiplier, i.e., no filtering is required for obtaining the answer, a problem handling capacity up to 5000 discrete problems per second with no loss in accuracy seems feasible.

AN OPERATIONAL-DIGITAL FEEDBACK DIVIDER

M. A. Meyer, B. M. Gordon and R. N. Nicola
Laboratory for Electronics, Inc.
Boston, Mass.

SUMMARY—The following article describes a device pable of finding the quotient of two numbers expressed in rallel binary code. Feedback type of operation is employed form a closed loop wherein the desired quotient is the only ssible steady state. The system response is similar to that an RC circuit. The associated time constant is directly oportional to the pulse rate involved. This device has been ccessfully applied in control circuits where system vari- les are actual numbers rather than more common voltages or rrents.

INTRODUCTION

In recent years there has been a trend toward wider pplication of digital techniques in control and data rocessing systems. These systems, in general, have een almost completely dominated by analog methods ostly because of readily available transducers which ave voltage or current representation of input quantities. ith the requirement of higher accuracy systems, digital ethods have come to the fore. In digital methods the imitation on accuracy is placed completely on the origi- al input measurement rather than on critical components f the control system. In these newer methods, the data ppears in the system as an actual number and not as a urrent, voltage or shaft position. The divider to be escribed in this paper is typical of the newer methods of chieving higher accuracy with fewer critical components nd in some cases much less total equipment. This di- ider in its original application was in a larger system mploying similar techniques throughout.

CHARACTERISTICS

To compete with existing analog systems, a digital nstrumentation cannot have a storage medium as found in general purpose digital computers. Such a storage medium would entail too much equipment and would remove the system from "real time." In this divider, input pulses operate directly on the output, so that, similar to analog operation, there is no delay in the system except for the inherent stray delays. It is this property of continuous and direct action that leads to the term "operational."

Another feature of this divider is the use of closed loop feedback type of operation. The output is continuously adjusted to follow the input by a comparison between existing and desired conditions. Use of this feedback eliminates errors due to transients or short time failures of components where as these errors would not be eliminated in an open ended system.

Finally, the accuracy of the system can be chosen by the user to match and maintain that accuracy that is inherent in the input to the system. It is not necessary to choose different components for different accuracies but merely to select the appropriate number of digits.

BLOCK DIAGRAM

The block diagram as shown in Fig. 1 indicates the functional operation. The dividend X is contained in register designated X, while the divisor Y is in register Y. The quotient Z is found in the forward-backward counter Z.

In operation, the numbers to be divided are read into registers X and Y. This can be done simultaneously and the input to these registers can be serial or parallel. It is not necessary to clear the forward-backward counter for any division nor is it necessary to halt the incoming pulse rate (F) during this read-in operation. After a time (to be discussed below) the number in the forward-back-

ward counter (Z) will be the desired quotient accurate to the nearest least significant digit.

The choice of the frequency of F will be discussed below. The two inputs labeled F should be time separate so that two pulses cannot arrive simultaneously at the

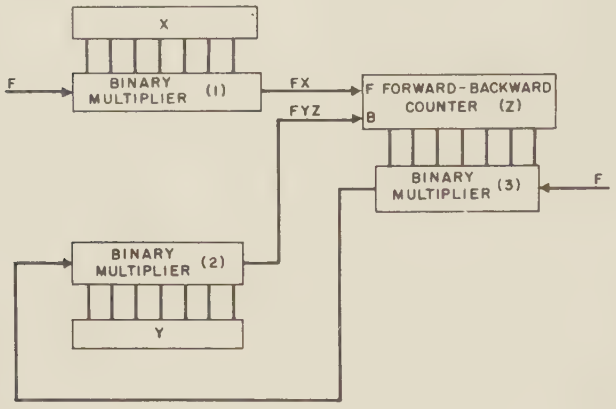

Fig. 1

input to the forward-backward counter. In systems where clock pulses are available this is no problem. If F is being generated in such a way that 180° phases are available, these will fulfill the requirement of time separation.

The binary multipliers[1] (BM) are shown in Fig. 2. A magnetic binary counter receives the pulses F, and each stage of this counter passes ½ of the number it receives to the crystal "and" gates which are rendered operative or are inhibited by the presence of a "1" or a "0" in the corresponding digit of the number in the parallel

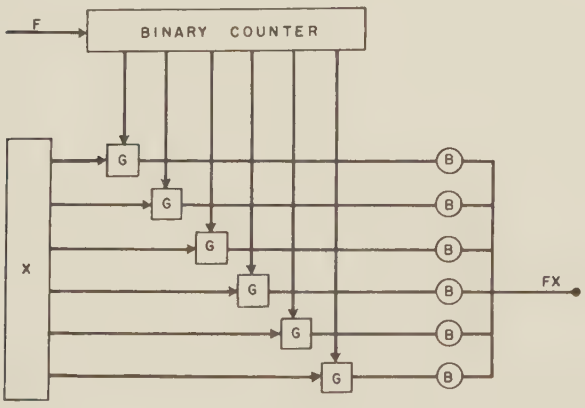

Fig. 2

register, in this case shown as X. Since the pulses out of each stage of the binary counter are selected at the non-carry time of that particular stage, the pulses going into the gates from any stage are time separated from the pulses of every other stage. In this manner simple crystal diode buffers (B) combine all the pulses that come through the gates back into a pulse train on one line. The number of pulses on this line is now the product of the input rate F and the binary number X. The register X can be any device which will contain a parallel binary code to indicate by one of two voltage levels the desired factor in the multiplication. In some applications X has been a magnetic shift register which was read out in synchronism with an output pulse from the binary counter.

Similar multipliers are used to obtain the products FZ and FYZ as shown in Fig. 1. The comparison in this loop occurs at the input to the forward-backward counter.

Fig. 3 shows the input operation. Assume that a backward pulse had arrived last. The flip-flop would then be in a reset condition and gate G_b would be activated (a pulse would pass). If a forward pulse now arrives, it does not pass through G_f and a small time later due to the delay D, it sets the flip-flop. The next forward pulse would then pass through G_f and trigger the least signifi-

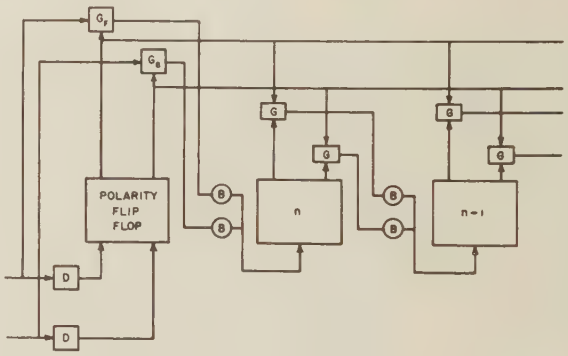

Fig. 3

cant digit of the forward-backward counter. On the other hand if a backward pulse had arrived after the first forward pulse, it would not have passed to the least significant digit. Arrival of alternate forward and backward pulses would not change the condition of the forward-backward counter. This would be the steady state condition. In effect, the error in the system must be greater than 1 least significant digit to cause a correction in the quotient Z. If either the forward or backward pulses are greater in number, the excess pulses will cause Z to change in a manner so that the number of pulses will become equal. The forward-backward counter is a common electronic type counter with gates supplied with carry pulses from each side of the particular counting stage. As shown in Fig. 3, these carry gates are actuated by the flip-flop at the input. In high speed applications simultaneous carry type counters must be used so that the delay in propagation down the counter stages does not exceed the time available before the arrival of the next pulse. In general, simultaneous carry counters are not needed since the time separation of pulses is large compared to propagation delays.

[1] B.M. Gordon and R.N. Nicola, "Special Purpose Digital Data Processing Computers", Proc. Assn. Comp. Mach., Pittsburgh Meeting; May 1952.

Fig. 4 shows a forward-backward counting stage uilt on a plug in unit. The unit shown is a high speed tage and uses a double triode plus cathode followers to rive the associated crystal gates.

ANALYSIS OF DIVIDER

As shown in the block diagram of Fig. 1, the forward-ackward counter receives two pulse trains. As a func-ion of time, the binary number contained in this counter an be expressed as:

$$Z(t) = \int_0^t \frac{XF}{2^n}\,dt - \int_0^t \frac{YFZ(t)}{2^n}\,dt \qquad (1)$$

here n is the number of digits of X, Y, and Z.

The positive integral represents the accumulation of orward pulses a period of time t, while the negative ntegral represents the accumulation of negative pulse ver the same period of time. Since the variable quanti-ies involved in (1) are discrete pulses, the variable t an only assume for its values integral numbers of input eriods of F. In other words, the smallest unit of time hat has any meaning is $1/F$. This must be so, since if he system and hence its related quantities change, it ust be with the arrival of a pulse.

Taking the derivative with respect to time of (1) ives

$$\frac{dZ(t)}{dt} + \frac{YF}{2^n}Z(t) - \frac{XF}{2^n} = 0. \qquad (2)$$

2) can be written as

$$\frac{dZ(t)}{X - YZ(t)} = \frac{F}{2^n}\,dt \qquad (3)$$

The solution of (3) is

$$-\frac{1}{Y}\,Ln\,[X - YZ(t)] = \frac{F}{2^n}(t + C_1). \qquad (4)$$

This can be written as

$$X - YZ(t) = C_2 \epsilon^{\frac{-YF}{2^n}t}. \qquad (5)$$

To evaluate C_2, the initial conditions must be known. o keep the solution general at $t = 0$, $Z(t) = Z(0)$.

Then C_2 can be found for a general case by substi-uting in (5).

$$C_2 = X - YZ(0). \qquad (6)$$

Substituting the value of C_2 into (5) gives the value of $Z(t)$ as a function of time.

$$Z(t) = \frac{X}{Y}\left[1 - \epsilon^{-\frac{YFt}{2^n}}\right] - Z(0)\,\epsilon^{-\frac{YFt}{2^n}} \qquad (7)$$

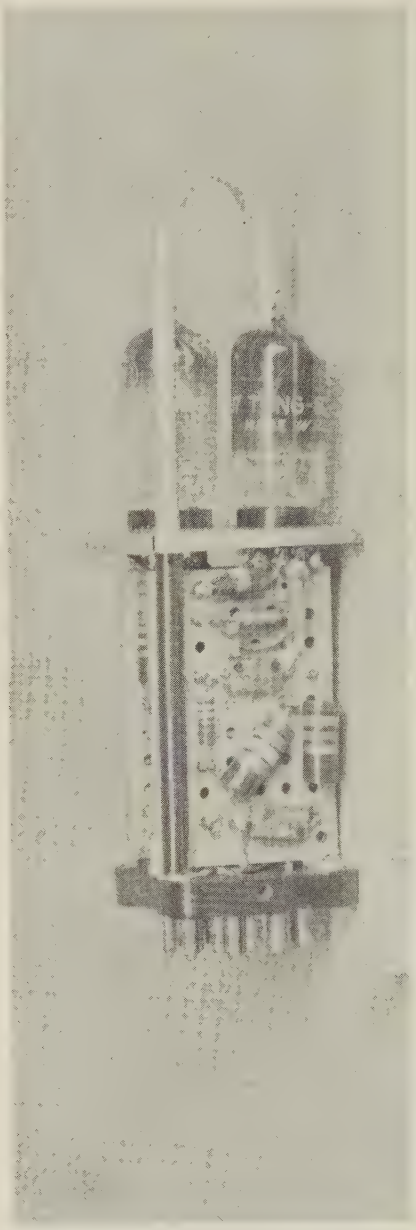

Fig. 4

From (7) it can be seen that as t increases, the negative exponential terms get large and the value of $Z(t)$ approaches X/Z, the desired quotient.

The form of (7) indicates the similarity of behavior to that of the voltage rise on a condenser in a simple RC circuit wherein the condenser had some charge on it at $t = 0$. The equivalent time constant of this loop is $2^n/YF$.

The interesting point is that the time constant can be adjusted by choosing the pulse rate F to achieve a time constant compatible with the particular application. A contrasting factor is that the time constant increases exponentially with the number of digits in the numbers to be divided. (7) also shows that if $Z(0)$ is nearly X/Y then the error is small even at $t = 0$. Such a situation would exist in a system where X and Y are changing slowly and do not vary at random as would be the case if pure arithmetic were being done.

The time required for the quotient to reach a desired accuracy can be calculated from (7). In this, as in any digital system, the maximum accuracy is one least significant digit. The quotient Z will be at its maximum accuracy when

$$Z(t_s) = \frac{X}{Y} = \frac{1}{2^n} \tag{8}$$

where t_s is the time required to reach the steady state.

Substituting the value of $Z(t_s)$ for $Z(t)$ in (7) gives

$$\frac{X}{Y} - \frac{1}{2^n} = \frac{X}{Y}\left[1 - \epsilon^{-\frac{YFt_s}{2^n}}\right] - Z(0)\,\epsilon^{-\frac{YFt_s}{2^n}} . \tag{9}$$

Taking the plus or minus error has no effect on the magnitude of the resulting value of t_s. (9) can now be simplified to

$$\frac{1}{2^n} = \left[\frac{X}{Y} + Z(0)\right]\epsilon^{-\frac{YFt_s}{2^n}} . \tag{10}$$

By the definition of a natural logarithm,

$$t_s = \frac{2^n}{YF} Ln 2^n \left[\frac{X}{Y} + Z(0)\right] . \tag{11}$$

(11) will give the time required to perform a desired division once the number of digits (n) have been specified and a pulse rate (F) has been selected. In order to take the worst possible case, the largest value of t_s, the worst combination of values of X and Y must be inserted in (11). This would be the case where Y is its smallest value, and X and $Z(0)$ are their maximum values.

To cite a particular case, assume that a desired system accuracy is 0.2%. In this case nine binary digits would be used. Assuming the worst values of X, Y, and $Z(0)$,

$$X = 511$$

$$Y = 1$$

$$Z(0) = 511$$

The pulse rate can be assumed at one megacycle. The time to reach steady state from (11) would be

$$t_s = \frac{512}{(1)\,(10^6)} \left[Ln\,512 + Ln\,1022\right]$$

$$t_s = 6.75 \text{ milliseconds.}$$

APPLICATIONS

This unit was developed initially for use in a system where the input quantity was measured in terms of two successively occurring pulse trains. The desired condition was that of equal numbers of pulses in each pulse train. These two pulse trains were fed into a counter which counted forward for the first group and backward for the second group of pulses. Anytime that this counter was left with a net number in it, this number represented an error. This error was to be used to actuate the system so as to tend toward equality in the two pulse trains. The difficulty arose in that the number of pulses that could be present in each pulse train could vary over a large range. Thus the amount of error was a function of the total number of pulses involved. This error then, which was the system actuation, had to be normalized so that in effect the loop gain would be constant. To accomplish this normalization, the forward and backward accumulations were done in register X while the total number of pulses was accumulated in Y. The system actuation was then taken from register Z.

Another application of this loop is to divide a frequency or pulse rate by time. This can be done by inserting a crystal or closely controlled frequency into binary multiplier 3. This same loop can also be used to determine the rate of change of a given pulse rate. This type of application is useful in radiation counting since the input quantity is already a pulse rate.

CONCLUSIONS

In its present form the whole unit is built with plug-in units so that the number of digits that are carried can be varied up to eleven digits. Until recently the pulse rates were limited by the magnetic counters to about 100 kc. At present, magnetic counters operating above 1 megacycle have been developed at the Laboratory for Electronics. If still higher pulse rates are required, electronic counters may be used in place of the magnetic counters thereby raising the possible pulse rates considerably.

CONTRIBUTORS

SAMUEL N. ALEXANDER was born in Wharton, xas, on February 22, 1910. He received the A.B. and S. degrees in Physics and Electrical Engineering from University of Oklahoma in 1931. He was awarded M.S. degree in Electrical Engineering from M.I.T. in 33, and from 1938 to 1940 he worked toward his Ph.D. M.I.T.

In 1940, and from 1945 to 1946, he was employed the Bureau of Ships to work on shipboard equipment, rticularly on electronic instrumentation. He joined ndix Aviation's Friez Instrument Division from 1944 1945, where he was senior project engineer on the velopment and design of electrical, magnetic and ctronic instruments. In 1946 he transferred to the tional Bureau of Standards. Here he helped to or- nize its digital computer development activity and s over-all supervisor of the design and construction SEAC, the first regularly operating electronic digital mputing installation in the U.S., for which the Elec- nic Computers Laboratory received the Commerce partment's Exceptional Service Award. As Chief of Laboratory, he has been technical representative to e Government agencies in the procurement of digital mputing installations and is presently supervising the gram for construction of DYSEAC and the design and velopment of a much larger machine, both for the partment of Defense. He has also acted as special nsultant on the application of electronic equipment the processing of routine paper work for such Govern- nt agencies as Bureau of the Budget, Treasury De- rtment, Social Security Administration, General Ac- unting Office and Bureau of Supplies and Accounts.

H. FREEMAN (A'49 M'52) received the B.S. de- e in Electrical Engineering from Union College in 46. From 1946 to 1948 he was a teaching assistant Columbia University, where he received the M.S. de- e in 1948.

In 1948 Mr. Freeman joined the Sperry Gyroscope mpany as a Project Engineer. He has been engaged the development of servomechanism, electronic com- ting circuits, analog computers, and guided missile stems. Since 1951 Mr. Freeman has been in charge of digital techniques development program including the sign of a general purpose digital computer. He was omoted to Senior Project Engineer in 1953.

Mr. Freeman is a member of the IRE, the AIEE, gma Xi, the IRE Subcommittee on Symbols for Feed- ck Controls Systems, and various IRE professional oups.

ALAN L. LEINER (M '54) was born in New York, Y., on February 10, 1914. He received the B.A. de- e from Yale in 1936. For the past 12 years he has worked in Government laboratories, – from 1942 to 1945 in the Navy Department and from 1945 to the present at the National Bureau of Standards.

During the war he participated in the development of the radio proximity fuze for non-rotating projectiles, and since the end of the war he has participated in the NBS digital computer programs which included the development of the general purpose digital computers, SEAC and DYSEAC.

In the SEAC program, Mr. Leiner was responsible for a major share of the logical organization of the SEAC computer. In the DYSEAC program he was in charge of the group responsible for planning the complete logical organization of the machine, i.e., formulating the logical specifications and designing and producing the detailed logical and pulse-signal wiring plans used in its construction. For the past two years he has also been concerned with a number of analytical study projects relating to the planning of large-scale digital data-handling systems for special business and military applications. As head of the System Design Group of the Electronic Computers Laboratory, he has also been concerned with developing effective methods for producing large scale logical and working plans for such systems.

BERNARD M. GORDON (A '49) was born in Springfield, Mass. on March 19, 1927. He received his B.S. and M.S. degrees in Electrical Engineering from M.I.T. in 1948. From 1948 to 1949 he was associated with the Philco Research Division where he was responsible for the design of a pole-zero analog computer. In 1949 he joined the Eckert-Mauchly Computer Corporation where he was project engineer developing acoustic memory systems, input-output equipment and control units of the UNIVAC.

In 1951, he became associated with the Laboratory for Electronics, Inc. where he was responsible for various digital control systems. Mr. Gordon is presently chairman of the Boston Section PGEC and instructs in computation and control devices at Northeastern University.

He has a comprehensive patent record and has published several papers in the computer field.

Mr. Gordon is a member of Sigma Xi, Tau Beta Pi and Etta Kappa Nu.

MAURICE A. MEYER (A '48) received a Ph. D. in Engineering Science and Applied Physics from Harvard University, and M.S. in Mathematics, and an S.B. in Electrical Engineering from M.I.T.

He worked on the development of IFF equipment at the Naval Research Laboratory and served in the U.S. Army Signal Corps in charge of ground radar reporting

stations. He has also served as an engineer on navigation systems at Wright Field and as engineer with Fada Radio Company and with Columbia Broadcasting System.

Dr. Meyer is at present Associate Director of Engineering at Laboratory for Electronics where he has been in charge of system design of automatic height finding radars and of an airborne navigation system. He has designed complex circuits for navigation systems, computers, feedback networks, receivers and MTI components.

RENATO N. NICOLA (S '48 – A '52) was born in Manchester, Conn. on July 5, 1923. He served in the U.S. Army from 1942-1946. He received a B.S. degree in engineering from the University of Connecticut in 1949.

From 1949 to 1951 he was an instructor in Electrical Engineering at Rutgers University. He received a M.S. degree from Rutgers University in 1951.

Since 1951 Mr. Nicola has been at the Laboratory for Electronics in Boston working on system and circuit design of an airborne computer with emphasis on development of magnetic components. He also worked on development of a magnetic matrix type of symbol generator.

Mr. Nicola is a member of the Association for Computing Machinery, the IRE and the AIEE.

EDWARD G. PARSONS (M '53) was born in Saratoga Springs, New York, on August 5, 1925. He received a B.S. degree in Electrical Engineering from Rensselaer Polytechnic Institute in 1950 and is currently doing graduate work in Applied Mathematics at Adelphi College.

Following his graduation, he joined the Sperry Gyroscope Company where he worked on the development of the time sharing analog multiplier presented in his paper in this issue. He later was concerned with the design of high gain feedback amplifiers for use in fire control systems. Presently he is engaged in the design and development of a general purpose digital computer.

Mr. Parsons is also a member of Sigma Xi, Tau Beta Pi, and Eta Kappa Nu.

REVIEW SECTION

It is the intention of this section to review articles that have been published since January 1, 1953 and to publish eventually reviews of all books of interest to those in the computer field. Articles dealing with electronic aspects of both analog and digital computers, as well as general expository articles, are to be included. All articles and books reviewed are numbered sequentially for each year; where known, the Universal Decimal Classification number is also given. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor.

GENERAL

.375.2 54-1

Can Machines Think?—M. V. Wilkes. *oc. I.R.E.*, vol. 41, pp. 1230-1234; tober, 1953; Reprinted from *Discovery* gland), vol. 14, p. 151; May, 1953.) fessor Wilkes approaches with cau- n the topic "Can Machines Think?" points out the difficulty in attempting assign a suitable definition of what l justifiably constitute definite dence of "thinking" on the part of a chine. He underscores the difficulties erent in the semantics of the prob- by stating that to some people the lity of a machine to pass a thinking lity test would prove only that the t was invalid, not that the machine ought." To this group, the concept "thinking" is reduced to something ch people can do and machines cannot thus making the whole subject a aningless one. Professor Wilkes gives hort description of a modern, intern- programmed, general purpose calcu- or, and shows that to ascribe the word inking" to the conditional transfer rations they contain is absurd. He s on to describe "learning" pro- ms which have been written for this n of machine, and points out that h programs provide the machine with arning" ability only in the precise egories that the learning program vides, and, thus, goes back ultimately the original programmer. Professor kes view is summed up by his tement, "What is wanted is a 'gener- ed' learning program which would ble the operator to teach the machine thing he chose, whether the idea of doing so had occurred to the pro- mmer or not." He concludes that such rogram has not yet been written nor it be written as an extension of the sent techniques, but he leaves open question of whether new methods provide this program or not.

M. J. Mendelson

54-2

An Application of Boolean Algebra to the Design of Electronic Switching Circuits—S. H. Washburn. (*Communication and Electronics*, No. 8, pp. 380-388; September, 1953.) A system of representing switching functions by Boolean algebra expressions is presented. Several instances are given where different circuits yield the same switching function. Considerable emphasis is given to the relationship between the assumed signs (positive or negative) of the individual signals and the "and" and "or" functions. Some of the problems encountered in sequentially acting circuits are described, and the steps in the design of a 3-pulse counting circuit are explained as an example. It is noted that the "and" function is represented by a "product" and the "or" function by a "sum" in contrast to certain earlier literature on the subject.

R. K. Richards

54-3

A Complex Algebra for Relay Circuits M. Raspanti. (*Elec. Eng.*, vol. 72, pp. 992-993; November, 1953.) Use is made of a relay circuit algebra developed by G. A. Montgomerie. This algebra takes into account the transition period between the opening of the closed contacts and the closing of open contacts. With some generalization of Shannon's fundamental relations, the concepts of symbolic logic can be applied to Montgomerie's algebra. A complex notation is introduced, and use is made of the fact that any contact circuit in series with a relay coil has the same effect as its negation in parallel with the coil. An example of the use of this algebra is given.

Harry T. Larson

621.316.54.512 54-4

Sketch for an Algebra of Switchable Networks—J. Shekel. (*Proc. I.R.E.*, vol. 41, pp. 913-921; July, 1953.) A combination of complex-number and Boolean algebra is outlined which can be applied in the analysis and synthesis of networks containing switches.
Courtesy of *Proceedings of the I.R.E.* and *Wireless Engineer.*

54-5

The Map method for Synthesis of Combinational Logic Circuits — M. Karnaugh. (*Communication and Electronics*, no. 9, pp. 593-599; November, 1953.) A method of finding the simplest 2-stage switching array for a given switching function is described. The method involves the use of a "map", which consists of a rectangle divided into a set of squares where each square represents one combination of conditions on the input variables. It is shown how the method can be used as an aid when the circuits are not restricted to the 2-stage variety. Further extensions of the method are applied to "don't care" conditions on the output line and to multi-output circuits. An example of a circuit for translating from the 1–2–4–5 code to the 2-out-of-5 code is worked out in some detail. Difficulties in using the method increase rapidly as the number of input variables is increased beyond four. Three-dimensional maps and other schemes for handling more than four variables are discussed.

R. K. Richards

ANALOG COMPONENT RESEARCH

621.385.2 54-6

An AM-FM Electronic Analog Multiplier—William A. McCool. (*Proc. I.R.E.*, vol. 41, pp. 1470-1477; October, 1953.) The multiplier described uses the adjuster-attenuator principle. A Foster-Seeley discriminator is the product-forming element. The modulation processes are stabilized with feedback. By making the information in the carrier amplitude proportional to the amplitude modulation index, four-quadrant multiplication is attained. An experimental model described has a center frequency of 1500 kc. The multiplier contains

This page has been left blank in order that readers may mount all reviews on cards.
— *The Editor*

even vacuum-tube envelopes, plus wer supplies and four chopper-stabil-ed dc amplifiers for multiplying two put voltages. Each additional multi-cand requires an attenuator contain-g four tube envelopes and two dc plifiers. The long term computing or was found to be within plus or nus one percent of full scale output. e author indicates that with further velopment this error could be reduced less than one-half percent. The usable ndwidth for both inputs is approximate-one percent of carrier frequency.

W. W. Soroka

8X621.375.2 54-7

The Magnetic Amplifier as an Analog mputer Element—Leonard J. Craig. roc. *I.R.E.*, vol. 41, pp. 1477-1482; tober, 1953.) The instrumentation used verify the ampere-turn relationship for parallel connected magnetic amplifier described. The magnetic material ed for the tests is characterized by an tremely low coercive force and is nergized by a regulated square wave wer supply. The result is a linear lation between the control signal and e pulse width of the output. Experi-ental data is presented for varying line ltage and load resistance as para-eters. Function generation circuitry is scribed to develop a phase sensitive lse width and a square wave phase ifter. Application to computers in the rm of an amplitude modulated D.C. ultiplier is instrumented with a bi-rectional modulator and a square wave ase shifter. Tests of the multiplier nstructed indicated that accuracies tter than 3.0 per cent could be hieved without the use of high preci-ion components.

J. A. Fingerett

21.375.2XR365.3 54-8

An Input-Output for Analog Com-uters—P. R. Vance and D. L. Haas. roc. *I.R.E.*, vol. 41, pp. 1483-1486; ctober, 1953.) A description of a device be used as either an X-Y recorder or s a curve-follower type function gener-tor. The drum uses 8½ by 11 inch aph paper to either record or play ack, using a special conducting ink. ertinent data are: drum peripheral elocity—10 inches per second; carri-ge—7 inches per second; input attenua-rs in 10 calibrated steps—from 0.50 mv r inch to 10 volts per inch. Static ccuracies are within 0.2 per cent of ll scale. The servo-amplifier system sed on the function generator essential-compensates for the dynamic and tatic errors of the servo. An example lustrating the use of the device as a nction generator for the evaluation of ourier coefficients of a periodic func-on is discussed and errors tabulated.

T. A. Rogers

54-9

Step-Switch Converter Digitizes Analog Data—R. R. Bennett and H. Low. (*Electronics*, vol. 26, pp. 164-165; November, 1953.) The Step-Switch Converter discussed converts an input voltage level to information which can be used to give a decimal indication of the input voltage value. The basic unit consists of a direct-current amplifier which compares the input voltage with a fraction of a 100 volt reference voltage supplied by a precision voltage divider and a telephone type stepping switch. The initially reset stepping switches step until the value of the input voltage is passed, and then stop. A second set of contacts on the stepping switch is used to energize the proper keys of a printer or may be used to give a visual type indication of the value of the input voltage. A relay amplifier senses the sign of the input voltage and energizes a relay which allows the printer to print plus or minus, as the case may be. This relay also selects for input to the basic unit either the original input or the output of a direct-current amplifier with an overall gain of minus one. Thus, the basic units receive as input the absolute value of the input voltage. The usable range of input voltage for this unit is plus or minus one hundred volts. The output is of two digit accuracy; however, more digits can be added by using more basic units.

Norman F. Loretz

54-10

A Progressive Code Digital Quantizer—F. Raasch. (*Communication and Electronics*, no. 9, pp. 567-571; November, 1953.) An analog-to-digital converter which operates through the medium of a "progressive" code is described. The progressive code is a decimal version of the Gray "reflected binary" code, and the object is to have successive digital quantities differing by only one digit. This property is in contrast with the familiar counting systems because, for example, the numbers 099 and 100 represent successive integers but the digits in each of the three positions have been changed. In the digital quantizer under discussion the individual bits within each decimal digit as well as the decimal digits themselves are arranged in a progressive code. Circuits are shown for converting an analog voltage to its digital representation in the progressive code. By means of an appropriate switching network (relays in this case) the progressive code can be converted to standard decimal notation. The system as built includes both visual and IBM punched card output.

R. K. Richards

ANALOG EQUIPMENT

54-11

Analog Computer Elements for Solving Non-Linear Differential Equations—Carl A. Ludeke and Cohn L. Morrison. (*Jour. App. Physics*, vol. 24, no. 3, pp. 243-248; March, 1953.) The authors describe a dynamic type for the solution of non-linear ordinary differential equations. The analog device consists of a small coil suspended coaxially in a magnetic field such as to act as a pendulum with a motion described by $A\theta + B\dot{\theta} + C\ddot{\theta} = 0$. The body of the paper describes methods used to vary c as a 1) function of time and 2) function of θ by variation of the current through the suspended coil. Current as a function of time was obtained from a mechanized potentiometer, current as a function of θ was obtained by controlling light to a photocell through a mask moved by the coil. Examples are discussed in terms of mask openings and response curves.

T. A. Rogers

54-12

A Coupling Analog for Non-Linear Systems with More Than One Degree of Freedom—C. A. Ludeke and R. T. Evans. (*Jour. Appl. Physics*, vol. 24, no. 2, pp. 119-122; February, 1953.) This paper was intended to follow the paper in the *Jour. Appl. Physics*, p. 243, March, 1953, and describes in detail a photoelectric coupling device for use with the Analog Computer of the March article. One or two examples are discussed.

T. A. Rogers

54-13

An Aerial Analogue Computer—W. Saraga, D. T. Hadley and F. Moss. (*Jour. Brit. IRE*, vol. 13, pp. 201-224; April 1953.) Problems of antenna-array design are discussed and a general expression for the field is derived on which the computer design can be based. A description is given of experimental apparatus, demonstrated in 1950 at the Physical Society Exhibition, by which the radiation pattern of a 2- or 3-element array is traced instantaneously on a cathode-ray tube screen. In array design, a satisfactory approximation to the required pattern is made by a direct method of curve fitting, the position of the elements, the current amplitude and phase being determined directly from the settings of the computer controls. Typical oscillograms are shown and explained. See (Brown and Morrison), page 1337, 1947 and (Todd); page 282, 1951.

Courtesy of *Proceedings of the I.R.E.* and *Wireless Engineer.*

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— *The Editor*

54-14

Resistance Network Analog Computer—(*Tech. News Bull. Nat. Bur. Stand.*, vol. 37, pp. 19-21; February, 1953.) The variant of the electrolytic tank analog for solving Laplace's equation in two dimensions, described here, uses, instead of a tank, a fine rectangular network of precision resistors. It is built to study axially symmetric electro-static fields for electron optics; hence, the resistances are not uniform but are graduated to give the potential in a radial plane in an axially symmetric field. It contains two arrays of sixty resistors in the axial direction by twenty resistors in the radial direction. Nodes corresponding to boundary electrodes of the field may be connected to any of twenty-five adjustable voltage sources; then the potential at any node can be read with a probe and a potentiometer which is accurate to one part in 10,000. Special terminal strips permit simulating the additional radial rows or making one axial end a plane of symmetry. This device, constructed under Dr. L. Marton, embodies improvements upon one developed by G. Liebman, (*Brit. Jour. Appl. Phys.*, vol. 1, pp. 92-103, April, 1950; and *Proc. I.R.E.* (London), Part IV, vol. 1, pp. 260-272; July, 1952.) However, details of the features are not given.

R. D. Elbourn

UTILIZATION OF ANALOG EQUIPMENT

54-15

Computer Simulates Moving Radar Targets—W. B. Birtley. (*Electronics*, vol. 26, no. 9, pp. 137-139; September 1953.) This article describes dual analog computers which simulate aircraft on radar indicators used in training radar fighter controllers. The speed and course of the interceptor and hostile aircraft presented can be altered by the radar operator and the radar instructor. The theory of operation is described and the necessary formulae derived. The physical operation of the computer is explained with reference to a block diagram showing the major components of the unit. Schematic diagrams of servo systems and the pulse-delay generator illustrate the electronic circuitry used in this equipment.

Norman F. Loretz

621.142 54-16

Hidden Regenerative Loops in Electronic Analog Computers—L. G. Peters. (*Trans. I.R.E.*, vol. EC-2, pp. 9; June, 1953.) This is a detailed analysis showing how coupling due to energy-storing elements gives rise to regenerative loops, the gain of which determines the system stability.

Courtesy of *Proceedings of the I.R.E.* and *Wireless Engineer.*

DIGITAL COMPONENT RESEARCH

621.375.2 54-17

The Design of Logical OR-AND-OR Pyramids for Digital Computers—S. E. Gluck, H. J. Gray, Jr., C. T. Leondes and M. Rubinoff. (*Proc. I.R.E.*, vol. 41, pp. 1388-1392; October, 1953.) Three methods are here shown for reducing the power consumed by diode gating circuits of the type used in MSAC, SEAC, MIDAC, FLAC, and DYSEAC. The first is to replace the pulldown resistor at the grid by resistors shunting the diodes of the or-circuit nearest the grid. The second is to feed the clock pulses directly into the and-circuits without intervening or-circuits (this has been done in FLAC and DYSEAC). And the third is to reduce all supply and signal voltages by a factor of five while keeping resistances the same. In combination these can reduce the power consumed by a factor of 50.

R. D. Elbourn

621.375.2 54-18

Dynamic Circuit Techniques Used in SEAC and DYSEAC—Robert D. Elbourn and Richard P. Witt. (*Proc. I.R.E.*, vol. 41, pp. 1380-1387; October, 1953.) A second type of logical circuitry competitive with the more widely used circuit elements based on the standard flip-flop is described by the authors. The new circuit techniques were originally developed for the SEAC (and later DYSEAC) digital computers at the National Bureau of Standards. Similar circuitry has since been adopted for such other computers as the MIDAC, FLAC and in England for the Elliott Brothers Computer. The basic aim of the new design is to develop a packaged, standardized type of circuitry. All logical operations are performed by a germanium diode resistor combinations; incidental storage is handled by electrical delay lines; and amplification is obtained by transformer-coupled pulse amplifiers using 6AN5 tubes. Two types of package, which may be produced by etched-circuit dip-soldered techniques, allow easy trouble shooting and offer complete generality in constructing logical functions.

J. W. Carr III

621.375.2 54-19

A Myriabit Magnetic-Core Matrix Memory—Jan A. Rajchman. (*Proc. I.R.E.*, vol. 41, pp. 1407-1421; October, 1953.) A high-speed, random-access memory for digital computers which has 10,000 tiny magnetic cores mounted in a square matrix of 100 rows and 100 columns is described. The cores are made of square-loop ferrite and each holds a single bit of information. A core is chosen by selecting the row wire and column wire which describes its position. A half-selecting current is then passed through each of these wires; the effect sums at the intersection to give that core a full switching current. Other cores in the matrix will receive at most a half-selecting current, and because of their square-loop nature they will not lose their information. A core is read by application of the half-selecting currents in a reference direction. The core either switches or it does not switch. If it switches, the flux change produces a voltage pulse on a sensing winding threaded through all of the cores in the matrix. If it does not switch, the voltage pulse does not appear. A sensing amplifier attached to the end of this winding will interpret the presence or absence of a pulse as the two information states of the core. Beside the desired signal, a number of unwanted voltages appear, which are integrated out over a complete memory cycle which includes rewriting the information. If the sensing amplifier recognizes that the core *did* switch, it modifies the rewrite part of the cycle so as to rewrite the information. The choice of one row out of 100 and one column out of 100 is made by a pair of 100-position magnetic-core switches made of small molybdenum-Permalloy cores mounted in 10 x 10 diamond-shaped arrays. With all 100 cores biased off, one row and one column are driven, switching the core at the intersection. This core is actually a nonlinear transformer, having a 16:1 turns ratio to provide the approximately 0.5-ampere pulse that is needed for the rows and columns of the 100 x 100 memory.

Dudley A. Buck

54-20

Stressed Ferrites Having Rectangular Hysteresis Loops—H. J. Williams, R. C. Sherwood, M. Goertz and F. J. Schnettler. (*Communications and Electronics*, no. 9, pp. 531-537; November, 1953.) The results of experiments relating to the behavior of ferrite cores under conditions of high radial pressure are presented. The pressure was applied by two different methods. With the first method a core was mounted in a special device in which a uniform radial force could be exerted hydraulically. In the second method the core was cast in a disc of plastic material which shrinks upon solidification. It was found that in the case of cores with negative magnetostriction the stressing produces substantial increases in the permeability and in the squareness of the hysteresis loop. Curves and data are shown which indicate the effects of variation in pressure, temperature, composition, and other factors. The cast plastic method of stressing is suggested as possibly being practical for computer applications; one core showed no change in magnetic properties after a period of six months.

R. K. Richards

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— *The Editor*

54-21

Pulse Response Characteristics of angular-Hysteresis-Loop Ferro-Mag- Materials – J. Wylen. (*Communi- n and Electronics*, no. 9, pp. 648- November, 1953.) The paper dis- es some of the factors affecting the e response of magnetic cores in- ed for digital storage applications. procedure and equipment are de- ed and output pulse shapes for n different metallic ribbon cores and ferrite core are presented. The rise of the applied current driving signal 0.4 microseconds in all cases. A le peak in the output was en- tered in several instances and us theories are suggested to explain phenomenon. In a discussion ap- ed by C. E. Ward it is suggested one of the two peaks is a con- ence of air leakage flux. The rtance of loading was mentioned, no data was given for loaded cores. , the paper did not extend to the e response problems encountered in cident-current memory systems.

R. K. Richards

396.615.17 54-22

Design of Triode Flip-Flops for Long- n Stability—J. O. Paivinen and . Auerbach. (*Trans. I.R.E.*, vol. 2, pp. 14-26; June, 1953.) This er presents a description of an ytical method of design based on siderations of dc stability, limiting rances in respect of voltage and ponent values being taken into ount initially. An Eccles-Jordan uit with injection diodes is con- red as a general case and equations derived expressing the operating ditions in the grid and the anode uits. Solution of these equations s appropriate key values. The hod is applied to three special es and a numerical example is given. esy of *Proceedings of the I.R.E.* and *less Engineer.*

.318.572:621.314.7 54-23

A Method of Designing Transistor gger Circuits—F. C. Williams and B. B. Chaplin. (*Proc. A.I.E.E.*, vol. , part III, pp. 228-244; pp. 245-248 cussion); July, 1953.) A fairly eral technique was developed after war for designing circuits that would rate with tubes having character- cs which varied within fairly wide rances, without component adjust- nts being necessary when tubes were nged. A similar technique is outlined point-contact transistors; this is ed on tube-circuit technique, and icularly on the analogy between the racteristics of transistors and pentodes. Basic pulse circuits considered include 2-state devices, timing circuits, counters and relaxation oscillators. Their application in digital computers is reviewed in detail.

Courtesy of *Proceedings of the I.R.E.* and *Wireless Engineer*.

R363X621.375.2XR282.12 54-24

A Transistor Pulse Amplifier Using External Regeneration—J. H. Vogelsong. (*Proc. I.R.E.*, vol. 41, pp. 1444-1450; October, 1953.) A regenerative transistor pulse amplifier, using a point-contact transistor, has been designed for operation in a synchronous serial computer with a 3 megacycle clock rate. The circuit is designed so that the clock input fixes the leading and trailing edges of the amplifier pulse output, making the output pulse shape practically independent of the waveshape of the trigger pulse. Both a trigger and a clock input are necessary to initiate the output; however, once the amplifier output is available, it is fed back through an external circuit to take the place of the initial trigger. Therefore, once triggered, the circuit is locked up through the external circuit until the clock pulse ends. The grounded-base configuration of the transistor is employed, since the use of external feedback eliminates the need of a large base resistance for regeneration. Six diodes perform the necessary gating functions for the trigger, feedback and clock pulses. DC restoration and impedance matching are obtained by using a transformer-coupled output. An ac input power of 12 milliwatts must be provided by the 3 megacycle clock. The transistor has a maximum dc dissipation of 50 milliwatts and 25 additional milliwatts are dissipated in the external circuit. Waveforms are shown with the amplifier working into a 500-ohm load and also into a load of four other amplifier circuits. Two difficult input circuits are compared in some detail and the pulse rise time for each circuit is calculated.

Donald J. Eckl

54-25

Thyratron-Vacuum Tube Counter—Richard W. Hofheimer. (*Electronics*, vol. 26, p. 198; November, 1953.) An explanation is made of a thyratron counter circuit improvement which eliminates the trouble encountered when both thyratrons of a conventional circuit conduct simultaneously. The replacement of one of the thyratrons with a vacuum tube and a revamp of the circuit accomplish the improvement. Schematic diagrams of both old and new circuits are given.

Norman F. Loretz

621.375.2 56-26

An Electromagnetic Clutch for High Accelerations—S. M. Oster and L. D. Wilson. (*Proc. I.R.E.*, vol. 41, pp. 1453-1455; October, 1953.) An electromagnetic clutch mechanism intended for the rapid starting and stopping of magnetic tape in computer systems is described. Basically, the mechanism consists of a friction disc which has one side in continuous contact with a rotating member and the other side in continuous contact with a stationary member. Through electromagnetic action the pressure is made great on one side or the other, and the output shaft is thereby caused to be rotating or stopped. The time required for acceleration from zero to 1,755 rpm with a 20 gm-cm^2 external load was reported to be 1.2 to 1.4 milliseconds including the time required for establishing the flux in the magnet. Descriptions of unidirectional and bidirectional models are presented.

R. K. Richards

681.142:016 54-27

Storage Systems in Arithmetical Computers—R. Dussine. (*Onde Elect.*, vol. 33, pp. 453-455; July, 1953.) Annotated references are given to 21 papers dealing with systems based on pulse counting, or on the use of (a) ultrasonic or electrical delay lines, (b) cr tubes, (c) magnetic materials.

Courtesy of *Proceedings of the I.R.E.* and *Wireless Engineer.*

R621.385.2 54-28

A Survey of Digital Computer Memory Systems—J. P. Eckert, Jr. (*Proc. I.R.E.*, vol. 41, pp. 1393-1406; October, 1953.) An historical approach is followed in treating about 40 different memory systems. Usually the principle of operation is described qualitatively, frequently priority is cited, sometimes qualitative comparisons are made, but only rarely are quantitative data or systematic comparisons given. The distribution of coverage is: one page to a dozen early devices including relays and ring counters; 2½ pages to acoustical, magnetostrictive, piezoelectric, and electrical delay lines; 4½ pages to electrostatic storage tube systems classified as surface redistribution, barrier-grid, holding beam, or sticking potential systems; one page to magnetic drums; and four pages to about 15 other systems mostly using discrete cells such as ferromagnetic, ferroelectric, capacitor-diode, neon-resistor, neon-capacitor, electrolytic diode, coherer and photoemissive-phosphorescent types.

R. D. Elbourn

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— *The Editor*

54-29
omputer Memory Uses Conventional Tubes—A. W. Holt and W. W. Davis. *ctronics*, vol. 26, no. 12, pp. 178- December, 1953.) In the electro- ic memory of the computer SEAC the lash method of F.C. Williams and T. urn is used to store 512 binary s on each of 45 cathode-ray tubes. use this memory is nearly three s old and over a dozen memories of same type are now in operation, a ialist in the field is not likely to anything new in this description; ever, a beginner should find it a eniently concise introduction to this s of high-speed memories. A theory ven for the charge transfer processes resulting potential distributions to unt for the dot and dash signals. A c cycle for sensing and rewriting spot in each of the 45 tubes re- es 12 microseconds. At least three of every four of these cycles are nerations and the other may be a or write. The timing of the memory als is given, along with the method ating for reading and writing. The plete system is described in block ram, and the chief requirements on lesign of each part are noted.

R. D. Elbourn

392.5:534.321.9 54-30
Ultrasonic Delay Lines—(*Electronics*, 26, pp. 210, 216; July, 1953.) This survey of the characteristics and ation of delay lines using fused- tz or glass rods with quartz- tal transducers.

rtesy of *Proceedings of the I.R.E. Wireless Engineer.*

54-31
The Status of Magnetic Recording—R. Zenner. (*Elec. Eng.*, vol. 72, pp. -954; November, 1953.) The author dis- ses the current state of the art of mag- c recording, including its faults and rtcomings. The majority of the engi- ring performed to date has been aimed excellence in sound recording. The igns thus developed are not neces- y useful in the newer fields of digital recording, physical analogue data ording and video recording. Such ters as frequency effects, phase ts, noise and long and short wave- gth effects are discussed. Carrier niques using amplitude modulation, uency modulation, and pulse-width- ulation are considered, and video ording possibilities are discussed.

Harry T. Larson

54-32
Magnetic Drum Design—D. G. O'Con- (*Electronics*, vol. 26, p. 196; No- ber, 1953.) This is a nomograph ch relates pertinent magnetic drum parameters in such a way as to determine the design features of a magnetic drum for a computer memory giving best compromise of cost, storage capacity and access time.

Norman F. Loretz

R365.35X621.385 54-33
Combined Reading and Writing on a Magnetic Drum—J. H. McGuigan. (*Proc. I.R.E.*, vol. 41, pp. 1438-1444; October, 1953.) This paper describes the use of a single non-contact magnetic recording head to read, alter if necessary and rewrite information in each cell of a magnetic drum as the cells pass at a 60-kilocycle rate with a cell density of 30 cells per-inch. It shows how the spreading of the writing flux around the head gap makes it possible to read the information stored in a cell before the cell reaches the position it occupied during writing on a preceding revolution, so that approximately two microseconds are available for logical decisions before rewriting is necessary. The reading circuit is required to disregard the pulse induced by writing in the preceding cell, and this requirement limits the cell density. The paper is excellent because complete circuit details with component values are given for the combined reading and writing amplifier, together with details of the circuit operation and of the results obtained. The paper is, therefore, immediately useful to a design engineer, and the techniques described will undoubtedly be adopted for other applications.

Paul L. Morton

54-34
Buffering Between Input-Output and the Computer—A. L. Leiner. (*Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conf., New York, N.Y., December 10-12, 1952*; pp. 3-7; March, 1953.) Buffering equipment is necessary for connecting a high speed computer and low speed, non-synchronous input-output equipment together. The buffering process includes pulse synchronization, assembly and transportation of words. Pulse synchronizing systems which produce a standard synchronized pulse for each incoming non-synchronous pulse are described. Methods of assembling digits into words, using precessing loops of delay line type registers and using shift registers, are mentioned. Transfer of words between pickup registers and high-speed memories may reqyire additional storage in the case that the high-speed memory is of the serial type. The transfer can also be accomplished by using the arithmetic register or reserved sections of the high-speed memory of the computer as buffer storage. For computers having serial delay line memories, concurrent computation and input-output operation without special registers can be achieved due to the fact that the computing facilities require access to the high-speed memory for only a limited percentage of the time, and the input-output rate is much lower than that of the internal memory. Regulation of information flow between the input-output equipment and the internal memory is essential, especially when a time-sharing concurrent input-output and computing scheme is employed.

T. C. Chen

54-35
Recording Techniques for Digital Coded Data—Arthur W. Tyler. (*Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conf., New York, N.Y., December, 10-12, 1952*, pp. 3-7; March, 1953.) This paper confines itself to a survey of techniques for recording coded data. Consideration is given to three phases of storage, namely: the recording technique, the mechanical recording medium, and the playback technique. There is constant mention of the limitation of system imposed by mechanical tolerances. Comparison of the storage densities realizable from the commonly used pulse recording systems are discussed. The photographic technique has been emphasized due to the paucity of published information on the subject. The characteristics of magnetic storage and punched tapes and cards systems are summarized. There is also a generalized discussion on the basic techniques now being used. This discussion includes mechanical, magnetic and optical techniques. The photographic process as applied to the recording of coded information is covered quite thoroughly. Photographic materials which can resolve 75,000 lines per inch, which is the limit of measurable resolving power, are available. At present it is practical to store about 100 spots per inch on film in the direction of film motion, and 50 per inch perpendicular to the direction of motion. Multiple channel recording and reproduction is simple because of the optical scanning technique available. The problems of dust particles, registration and reading and recording techniques are covered, together with a discussion of the practical problems associated with the design and operation of the equipment. The techniques used are also applicable to reading spots on tape recorded with printing equipment. Such systems have the advantage of high-storage density, moderately high recording rates, visibility for inspection and low cost. The possibility of storing ten million bits of information on a 6" diameter glass disc mounted on suitable bearings is discussed. Such a disc coated with

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— *The Editor*

tographic emulsion could store, 00,000 bits per square inch. The 6" would contain the same storage that be realized with 150 feet of 35 mm or 750 feet of ten-channel magnetic e.

Harry Kenosian

54-36

Devices for Transporting the Record-Mediums—R. L. Snyder. (*Review of ut and Output Equipment Used in mputing Systems, Joint AIEE-IRE-M Computer Conf., New York, N.Y., cember, 10-12, 1952;* pp. 15-21; March, 53.) The requirements of recording terial and transport devices are ien. The advantages of binary code r decimal notation as well as some cking codes are mentioned. The ious types of recording systems cussed are: 1. Perforated tapes. The es are perforated by punches and d by mechanical feelers or photo-ctric devices. 2. Punched cards. nched card system is capable of nsferring 400 decimal characters per ond. 3. Photographic recording. Pat-ns on cathode-ray tube are recorded photographic film which is then anned photoelectrically for repro-tion. 4. Magnetic recording. Magnetic e, wire and drum are used for the ording media. Types of tape trans-t devices are described. 5. Prepara-n devices. Manually encoded data are pared on standard tape-punching or d-punching key boards. 6. Printing vices. Automatic typewriters have dequate speed, but high-speed ctromechanical gang printers are sidered to be fast enough to keep e with the fastest computer.

T. C. Chen

54-37

Quarterly Report No. QW — John R. wman, F. A. Schwertz, et al. (*Quart. pt. Computer Components Fellowship llon Inst.,* 205 pp.; July 11, 1953 - tober 10, 1953.) The Quarterly Pro-ss Report No. 12 contains nine ctions as follows: I. Bistable Optical ements II. Electroluminescence III. otoconductivity and Electrolumines-nce IV. Electrical and Optical Proper-s of Silicon Carbide, V. Printed cuitry via Xerography, VI. Circuit brication — Capacitor Sheets VII. urable Transformers as Gates VIII. gital-to-Analogue Converter IX. Com-ter Components Research at Mellon titute. Section I contains some ormation on the problems and tech-ues involved in fabricating a binary it storage tube comprising a photo-hode and a phosphoranode in an acuated glass envelope. Section II tains data relative to the construc-n and testing of two-dimensional ctroluminescent light sources. Section contains some information concerning feasibility of using the phenomena of photoconductivity and electroluminescence for storage and switching purposes. Section IV has to do with the rectification and light-emitting properties of point contacts on silicon carbide crystals. Section V comprises a report on some experiments designed to determine the feasibility of employing the Xerographic printing technique for the fabrication of printed circuits. Section VI presents an account of some experiments in which capacitors were materialized by spraying conducting silver paint on flat sheets of barium titanate ceramics. Some experiments employing (non-square loop) ferromagnetic ferrites as switching and gating elements are described in Section VII. Section VIII contains a description of a digital-to-analogue converter which decodes the number in a counter or register by means of a linear resistor network in such a way as to yield an analogue voltage proportional to the number. Section IX contains a summarized account of the Mellon Institute work on computer components.

F. A. Schwertz

DIGITAL EQUIPMENT

621.375.2 54-38

SEAC — Sidney Greenwald, R. C. Haueter and S. N. Alexander. (*Proc. I.R.E.,* vol. 41, pp. 1300-1313; October, 1953.) A description of the logical, electronic and physical characteristics of a large scale digital computer called the SEAC is given in this article. The authors have presented the more general aspects of the machine in block diagram form and in addition have given pertinent illustrations of the instrumentation of the logic. A brief description of the operating characteristics, including the optional three or four address code, is followed by a large detailed section on machine organs. The basic philosophy of the circuit design is presented in detail and the physical construction that resulted from these techniques is briefly described. The article concludes with a section on operating performance which includes general information on maintenance, programming checks, and type of problems the SEAC has successfully handled.

S. E. Gluck

54-39

The Electronic Computer at the Institute for Advanced Study—Gerald Estrin. (*MTAC,* vol. VII, pp. 108-114 and frontispiece; April, 1953.) This article describes the all-electronic, general purpose digital computer at the Institute for Advanced Study in Princeton, New Jersey. The machine characteristics are outlined, followed by descriptions of structure, memory, arithmetic and control operations, and a short note on operating experiences since June 1952. The machine seems to be a close forebear of the IBM 701. It is a one-address, binary, parallel machine with 1024 40-bit words of Williams' type memory. The memory has a 24 μsec. period and a read-around ratio of about 30.

John Selfridge

54-40

A Special Purpose Digital Computer—J. P. Walker, Jr. (MTAC, Vol. VII, pp. 190-195 and frontispiece; July 1953.) This article describes a computer for the solution of 1200 or less simultaneous linear algebraic equations by the Gauss-Seidel iteration method. To save storage space, only the non-zero coefficients are stored. These are stored on a continuous loop of multi-channel magnetic tape. The current iterates of the unknowns are stored on a magnetic drum which revolves at about 3500 rpm. The arithmetic section operates on floating binary numbers with 20 digits for the number and 5 digits for the exponent. Addition time is 200 μsec. and multiplication-division time is 40 addition times. End-around-carry and "one's" complements for negative numbers are used. There are about 400 plug-in type components, designed to require a 15-20 volt positive pulse input, and to operate reliably over wide variation of supply voltages and tube characteristics. The computer has solved a set of 793 equations by making 15 iterations of 20 minutes each.

John Selfridge

621.375.2 54-41

The Design of the Bendix Digital Differential Analyzer — Max Palevsky. (*Proc. I.R.E.,* vol. 41, pp. 1352-1356; October, 1953.) This article is a description of the characteristics of the Bendix Digital Differential Analyzer, principally from the viewpoint of mathematical analysis and mechanization. Although generally similar in nature to other digital differential analyzers the Bendix version has incorporated two fundamental changes in the manner in which it handles the integration process. The first of these provides a trapezoidal form of integration instead of a simple linear form. The second provides an output means for each integrator so that its incremental outputs are recorded and transmitted to other integrators as a $+1$, -1, or 0 signal. This is in contrast to the other versions of this type of machine in which outputs are of the form $+1$ or -1. In the latter form zero is represented by an alternating stream of outputs of the form $+1, -1, +1, -1, +1, \ldots$ The paper presents heuristic arguments to substantiate the Bendix claim that these

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— *The Editor*

changes produce higher accuracies. The paper shows that the Bendix Digital Differential Analyzer has included several features new to this form of computer and has eliminated some others available in other mechanizations. The Bendix version makes provision for the automatic varying or resetting of initial conditions as a problem is being run. With this flexibility a technique has been developed for the automatic handling of two-point boundary problems. The methods employed in the Quadratic Arc Computer for automatic function interpolation have been embodied in the Bendix Digital Differential Analyzer to provide for empirical or arbitrary function generation by means of a second order interpolation process. Step functions may be automatically entered. The computer may be filled from paper tape. Output is by means of an electric typewriter and proceeds in parallel with computation. No indication is given that curve follower input or curve follower output is available.

M. J. Mendelson

621.375.2 54-42

The Logistics Computer—R. S. Erickson. (*Proc. I.R.E.*, vol. 41, pp. 1325-1332; October, 1953.) A general description of the Logistics Computer is presented. The purpose of the computer is to perform relatively simple calculations on large amounts of data. Fixed sequence programming is employed, using a plugboard to specify the desired program. The machine uses the excess three binary coded decimal system, with negatives expressed as nine's complements. Input-output is accomplished either by punched tape at ten characters per second or by magnetic tape at speeds up to 600 characters per second. Magnetic drum storage of 180,000 decimal digits is available, with a basic pulse rate of 220 kc. Basic circuits are constructed on plug-in chassis, with each chassis accommodating up to 22 tubes or similar components. The entire computer is enclosed in air-conditioned cabinets. Provisions for marginal checking are built into the machine. Special controls are also provided to allow slow speed or step-by-step operation for diagnostic checks.

Vernon C. Kamm

54-43

Converters Between Teletype Tape and IBM Cards—Glen F. Nielson. (*Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conf., New York, N.Y., December 10-12, 1952;* pp. 11-14; March, 1953.) Characteristics of the (IBM) type 63 card-controlled tape punch and type 43 tape-controlled card punch are discussed. The two machines are designed to interchange information between punched card systems and teletype tape input-output equipment. The type 63 consists of a card-reading unit and a tape-punching unit which operate to perform the following functions: 1. Sense information on cards. 2. Analyze and convert the 12-unit card code to the 5-unit telegraphic code. 3. Punch the information into a paper tape at the rate of ten characters per second. A pluggable control unit provides flexible control to supplement the built-in automatic control features. The sequence of information on the card must be the same as that desired on the tape. Columns can be skipped or inserted by control panel wiring. The type 43 tape-controlled card punch comprises three units: the card-punch unit, the tape-reading unit, and the keyboard unit. The keyboard, which is optional, provides manual card punching which can be used either concurrently with the tape reader, or independently. The three basic machine operations are the same as for the type 63 unit. All machine operations are controlled by a pluggable panel. Tape reading and card punching speeds are ten columns per second.

The paper tape used is $^{11}/_{16}$" wide and .003 inches thick.

Harry Kenosian

621.375.2 54-44

The Remington Rand Type 409-2 Electronic Computer — Loring P. Crosman. (*Proc. I.R.E.*, vol. 41, pp. 1332-1340; October, 1953.) A brief description of the machine named in the title — a plug-board programmed, card reading and punching computer — is given, together with a logical organization chart and a number of illustrations of component parts. A decade unit which is unusual in that it counts in either direction, the accumulator, and the decimal computer are discussed functionally. Input and output to the three types of storage, card, constant switches and intermediate result relays, are described and the barest minimum of speed and capacity information is given. Short sections on a self-checking feature (based on redundant computations), a card reproducer, service features, and programming conclude the paper, one clearly intended to be merely an invitation to the curiosity of the reader.

J. Weizenbaum

621.375.2 54-45

The Arithmetic Element of the IBM Type 701 Computer—Harold D. Ross. (*Proc. I.R.E.*, vol. 41, pp. 1287-1294; October, 1953.) The author describes very clearly the entire arithmetic element of the IBM 701 with emphasis on the basic arithmetic storage unit, and on the operation of addition. The basic arithmetic storage unit is a one microsecond delay rather than the commonly used Eccles Jordan flip flop or magnetic cores. The input to the delay unit is a dc signal of either +10 or −30 volts. This signal is sampled by a .35 μsec. sync pulse every microsecond. If coincidence occurs, the coincident pulse energy is stored in a condenser which in turn produces a dc output of the same level as the input one microsecond later. The delay unit will function as a flip flop by merely gating the output back to the input. Some advantages of this delay unit are that the input can be switched during the .6 μsec. period between sync pulses, and that it facilitates the use of dc logic thus simplifying the circuitry. The delay unit circuit and block diagrams are shown. Addition is performed by using a parallel binary adder. Multiplication is performed by repeated addition, and division by repeated subtraction of the restoring type; however, restoration is not necessary because of a particular feature of the adder.

Hubert M. Livingston

54-46

A Subscriber Toll Dialing Tape Reader—W. H. Blashfield. (*Elec. Eng.*, vol. 72, p. 786; September, 1953.) This paper is a short (1 page) description of the functions accomplished by a tape reader adapted to telephone toll dialing operations. Briefly, the tape reader translates the holes punched in a tape which was prepared automatically by the telephone system to a readable form on a toll ticket. Means are included for calculating toll charges.

R. K. Richards

UTILIZATION OF DIGITAL EQUIPMENT

54-47

The Use of Large Scale Computing in Physics — J. Sheldon and L. H. Thomas. (*Jour. Appl. Physics*, vol. 24, no. 3, pp. 235-242; March, 1953.) After listing the major high speed computers now in existence, a brief description is given of the numerical methods available for solving some of the standard partial differential equations of mathematical physics. Estimates are given of the number of operations required to treat these equations in one to four dimensions. In terms of these estimates, an appraisal is given of the suitability of "typical" computers of varying characteristics for handling such problems. Finally, there is presented a "brief description of seven typical computations . . from the published literature". Two minor deficiencies may be noted in this otherwise excellent article. First, most of the emphasis is on boundary value problems — very little is mentioned about eigenvalue problems. In particular, the recent techniques developed for finding the eigenvalues of matrices are not mentioned. Second, references to the published literature are on the scanty side and most references cited date back three or four years. This is rather a long time for a rapidly developing field.

David Saxon

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— *The Editor*

54-48

Diagnostic Programming Techniques the IBM Type 701 E.D.P.M. — L. R. lters. (*Conv. Rec. I.R.E., 1953 Nat. nv., Part 7*, pp. 55-58; 1953.) Pro- ms for analyzing and isolating nponent failures are described and advantages of such programs over ensive test equipment are pointed . These programs must be designed that failures in the component being ted, e.g., arithmetic or memory, will cause the program itself to fail. Such grams are especially suitable for the because of its directly-coupled line nter which permits constant monitor- and which presents test results idly. Diagnostic programs are used in junction with marginal testing and supplemented by self-checking grams designed to aid in diagnosis well as detection of errors. Diag- tic programs for testing electrostatic mory and tapes are described, the er employing center-square random bers.

John R. Lowe

54-49

Floating Operations on the EDSAC — A. Brooker and D. J. Wheeler. (*MTAC*, l. VII, pp. 37-46; January, 1953.) The ficulties which arise when program- ng calculations for large automatic culating machines which have a fixed cimal point are discussed. This leads a consideration of the possibility of ng floating decimal arithmetic for tain kinds of calculations. A method which floating decimal arithmetic can carried out with any fixed decimal- nt machine is outlined, and the heme adopted for use with the EDSAC described in detail. This scheme is sed on a special kind of subroutine led *interpretive*. This enables the grammer to use a new order code of own choice. The 'orders' of a pro- mme drawn up with such a code are ected under the action of the inter- tive subroutine and interpreted in ms of sequences of orders which form the required operations. With EDSAC, a single address 'order' de has been adopted, similar to the inary order code, in which the thmetical 'orders' are interpreted in ms of floating decimal arithmetic. cial 'orders' for simplifying counting erations and the modification of other ders' are provided. The 'order' code described in detail and an example is en of a programme drawn up using s code. Other topics discussed are use of auxiliary subroutines with the erpretive subroutine, a method of ilitating programme assembly, and hniques for using the input tape as a m of auxiliary store. Finally the es of operation of the individual 'orders' of the code are given, together with an estimate of the factor by which the calculation time is increased as a result of using floating decimal arithmetic for an entire calculation.

R. A. Brooker and D. J. Wheeler

54-50

The Use of a 'Floating Address' System for Orders in an Automatic Digital Computer — M. V. Wilkes. (*Proc. Camb. Phil. Soc.*, vol. 49, part 1, pp. 84-89; January, 1953.) This paper describes the form in which floating addresses were originally conceived by the author. The idea has since been developed and used extensively at M.I.T., and elsewhere. It consists of referring to instructions, when writing them, not by their addresses but by labels which are written in as required by the programmer. The machine must perform a conversion after input, before the program is ready to be used, but advantages are gained in the ease of writing and correcting programs. A routine for performing the conversion is shown, with an example of its application. As given here, floating addresses appear somewhat clumsy to use as they were added to the existing scheme for writing programs for the EDSAC; later forms have been more convenient. The author illustrates how the use of floating addresses makes short open subroutines attractive, especially if they are copied into the program by the machine itself during loading. They can then be represented in the written copy by groups of symbols which the author calls 'synthetic orders'.

Stanley Gill

54-51

Compiling Routines — G. M. Hopper. (*Computers and Automation*, vol. 2, no. 4, pp. 1-5; May, 1953.) Programming constitutes a serious bottleneck in computer operation, in both time and accuracy. A very promising solution to this problem lies in the principle of setting the computer to program itself. The technique of using subroutines to perform operations that are not built into the computer is used almost universally. Automatic incorporation of these subroutines into larger programs can be effected in two ways: (1) the interpretive method, in which a subroutine is set into a fixed memory position and the appropriate modifications, data transfers, and control transfers made; and (1) the compiling method, in which the subroutine is copied into the main routine. With either method it is possible to construct "pseudo-codes," in which mathematical functions are represented by single computer words. The reduction in programming time is tremendous. The extension of these principles to non-mathematical applications looks very promising, although some standardization in notation will be necessary. Even this standardization can be made automatic.

R. Lipkis

621.375.2 54-52

Fundamentals of Digital Computer Programming — Walker H. Thomas. (*Proc. I.R.E.*, vol. 41, pp. 1245-1249; October, 1953.) This paper presents fundamental concepts of programming for a general purpose computer of the stored program type. The author describes the basic elements necessarily present in such a device and creates a simplified machine containing all of these elements. By means of this simplified machine he describes the sequence of operations which a computer performs in executing the various commands which its designer has given it. He then proceeds to show by a series of examples how a programmer can make use of this basic computing ability to produce more complex operations. Each example is simple in nature and is intended to show one particular aspect of programming. The paper stays at a very fundamental level at all times. It is recommended for those who wish a good non-technical introduction to the concepts of computer structure, operation, and programming.

M. J. Mendelson

ORIENTATION READING

54-53

Keynote Address—Norman H. Taylor. (*Review of Input and Output Equipment Used in Computing Systems, Joint AIEE-IRE-ACM Computer Conf., New York, N.Y., Dec. 10-12, 1952;* pp. 1-2, March, 1953.) This keynote address discusses the input-output equipment philosophies associated with three types of digital computing systems. These include the scientific calculator which performs a large amount of calculation from a small amount of input data. The time consumed in the operation of the calculator represents a considerable proportion of the time required for inserting a problem and receiving printed answers, so that comparatively slow input-output equipment does not impair the machine efficiency. The second system discussed is the business machine systems, which require comparatively simple operations on large amounts of data, and must produce large quantities of output data. In such systems, the internal calculator can process data faster than the data can be fed in or read out, so that a serious problem exists in developing input-output equipment capable of matching the speed of the internal calculator.

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— *The Editors*

techniques used to solve this
lem include buffer techniques using
mediate storage and parallel opera-
The third system is the automatic
roller, in which the internal calcu-
must be able to accept data and
results for operating mechanisms,
h conditions will require input-
ut equipment which will match the
to and from the controlled machine
internal calculator. In all three
ems, there are two basic points of
which are diametrically opposite.
point of view tends to adopt input-
ut equipment operations to the
nal calculator, the other point of
calls upon the internal calculator
eep the data fed to it flowing for
mum efficiency between the input-
ut terminals.

H. Kenosian

54-54

Will Machines Replace the Human n? — Serge Fliegers. (*American ury*, pp. 53-61; January, 1953.) This le was not aimed at a technical ence and accordingly contains ing of technical interest. Where it hes up against the technical facts, ontains the usual number of mis- ements and errors found in "popular" les. It also contains the usual ber of "human interest" anecdotes extravagant statements designed to coax the lay reader from one paragraph to the next. The question posed in the title is not answered in the context.

F. A. Schwertz

BOOK REVIEWS

54-55

Proceedings of a Symposium on Industrial Applications of Automatic Computing Equipment — (*Midwest Res. Inst., Kansas City, Mo.*, 191 pp.; January, 1953.) In these proceedings are several articles which serve as an excellent description of the usefulness of computing machines to engineering design. Desk calculators, analog computers, differential analyzers, IBM punched card and Univac machines are all treated in articles describing the problems of installation, maintenance and operation of the equipment. A third group of articles gives details of various applications. In discussing analog computers, the principles of application to control problems are described. Some of the types of problems discussed in detail, in regard to programming, cost, volume, etc., are: solution of systems of linear equations; integration of partial-differential equations, distillation-equipment design, gear design. Many other engineering problems are given brief mention.

Courtesy of *Appl. Mech. Rev.*

G. W. King

54-56

High-Speed Computing Devices — C. B. Tompkins, J. H. Wakeling and W. W. Stifler. (McGraw-Hill Book Co., Inc., New York, N. Y. 451 pp., diagrams, charts, tables; 1950.) This book was first assembled in a report to the Office of Naval Research and is one of the few volumes devoted to the rapidly growing field of high-speed computing machines. It is divided into three broad sections covering the philosophy and basic elements of machine computation, computing systems and physical components. The prime emphasis is on digital computation systems although one chapter is devoted to various kinds of differential analyzers and other analog computing systems. Each chapter has a large bibliography. Two chapters are devoted to arithmetic systems and numerical analysis. Desk calculators, punch-card computing systems are described. Brief descriptions of the large-scale digital computing-machine projects in the United States are also given, including a statement of some of the problems which have been programmed on these machines. Several methods of dated conversion and storage systems are discussed. The advantages and disadvantages of various storage systems are quite completely summarized. The book is, in fact, almost an encyclopedia of the present methods in use in the field.

Courtesy of *Appl. Mech. Rev.*

N. B. Nichols

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